

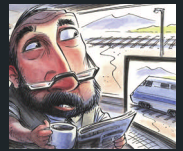
# EDN

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SEPT

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Issue 17/2009  
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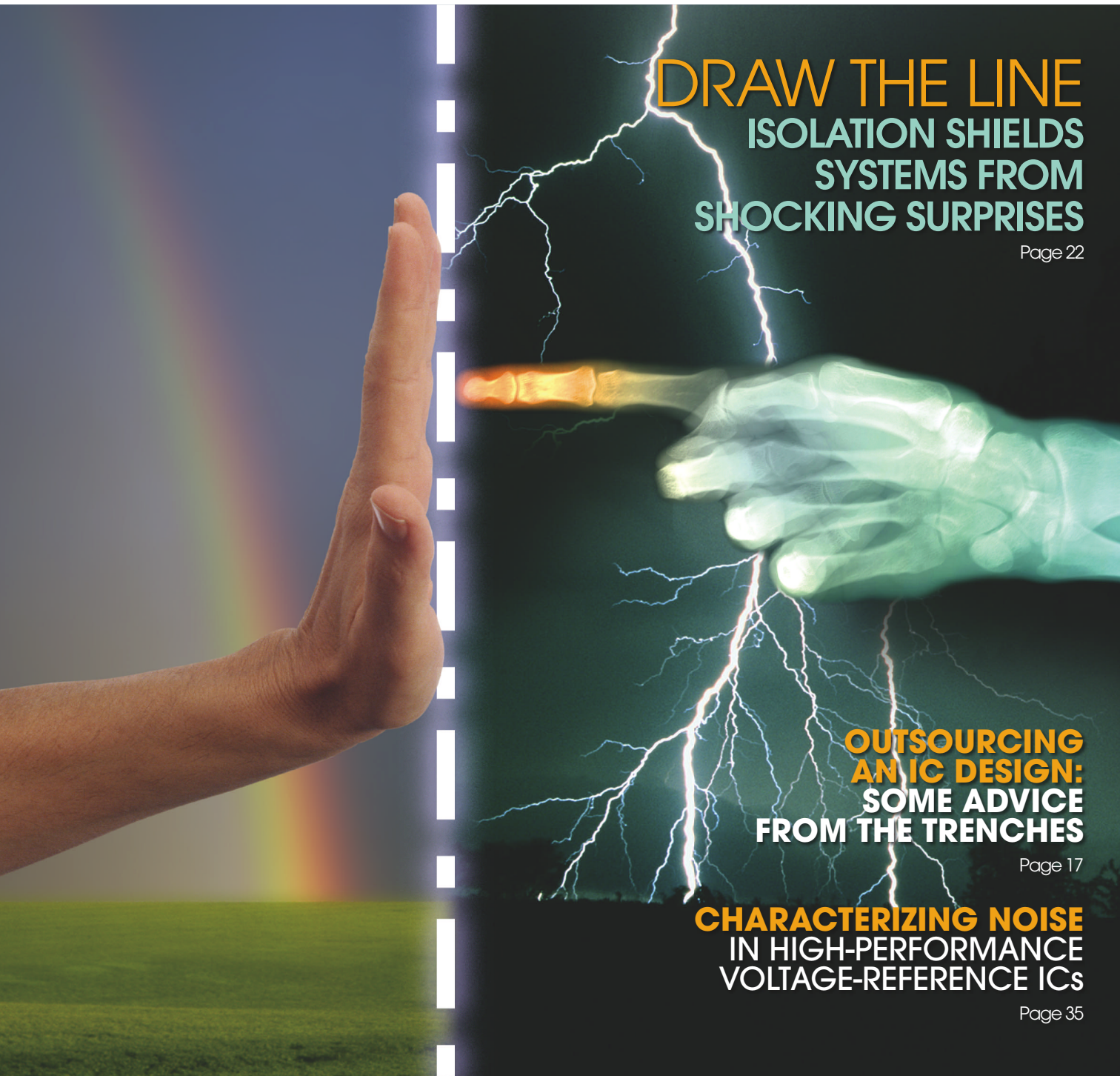
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## DRAW THE LINE

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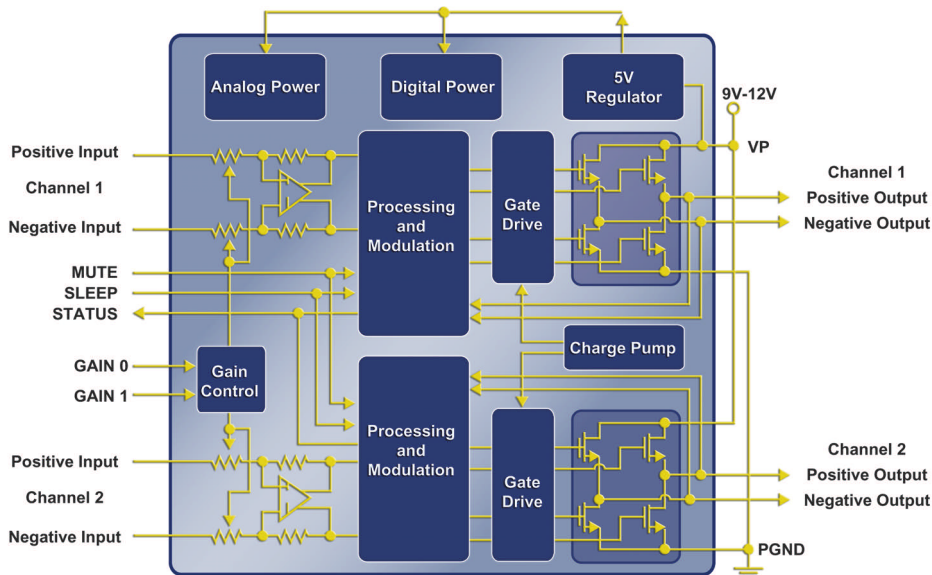
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# innovation



## CS3511

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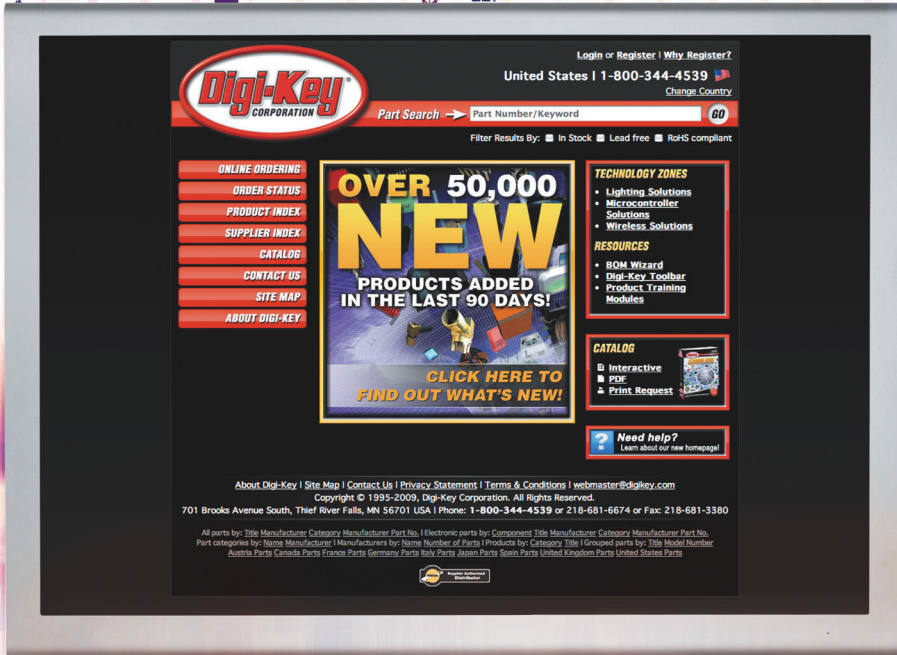
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# MEET THE GUY that ELIMINATED HIS TEAM'S MANUFACTURING VARIABILITY ISSUES.



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## Draw the line: Isolation shields systems from shocking surprises

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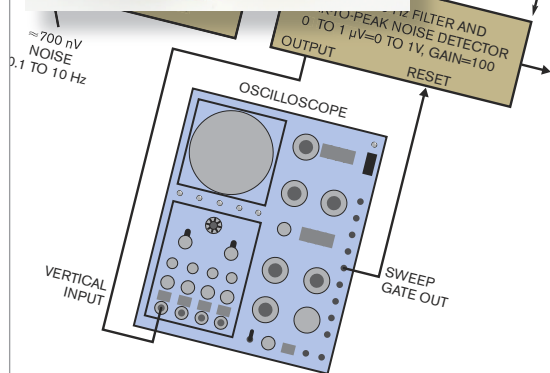
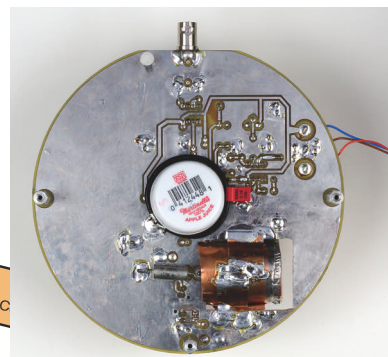
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Dilbert 10

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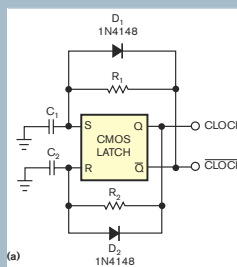
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# Welcome to the World of Mixed-Signal FPGAs



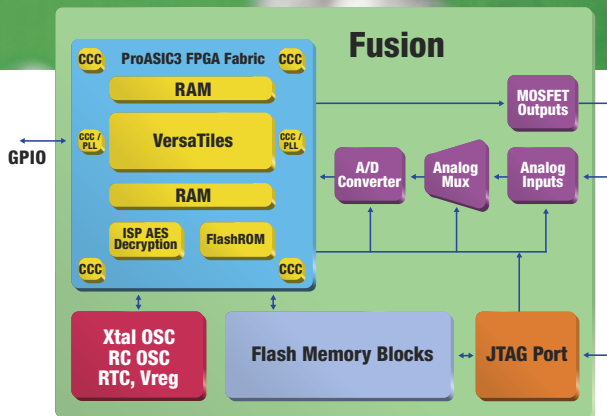
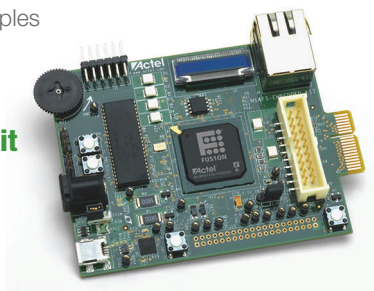
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- PCB schematics, layout files, and BOM

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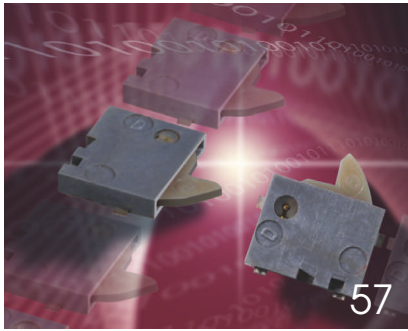


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**EDN** online contents

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### ONLINE ONLY

Check out these Web-exclusive articles:

#### Understanding power-over-Ethernet power allocation

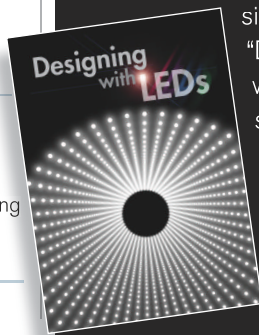
Along with the growing popularity of POE (power over Ethernet) has come growing demand for intelligent and efficient POE power allocation and management. In response, today's POE-silicon suppliers have made sure that real-time power management is an integral part of virtually every enterprise-grade midspan and switch. Still, confusion about power-allocation best practices persists. [→www.edn.com/article/CA6675387](http://www.edn.com/article/CA6675387)

#### Use simultaneous-sampling ADCs to monitor three-phase ac-line power

Multichannel simultaneous-sampling ADCs trim your costs and simplify power-monitoring systems. [→www.edn.com/article/CA6677015](http://www.edn.com/article/CA6677015)

### Lighting for the 21st century

Practical, inexpensive HB LEDs (high-brightness light-emitting diodes) are here. Now, what can we do with them, and what will be their impact on electronics and consumers? Read more in the online version of EDN's "Designing with LEDs" supplement. [→www.edn.com/article/CA6650340](http://www.edn.com/article/CA6650340)



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BY PAUL RAKO, TECHNICAL EDITOR

## In a downturn, treat your customers right

**W**hen things are bad, as they are now, smart companies know enough to treat their customers right, even if the customer is wrong. As an example, 15 years ago, I started having trouble with an 8-foot fluorescent fixture in my shop. I went to my nearby hardware store, Orchard Supply Hardware, and bought a new ballast. After I used it to replace the ballast in my fixture, I turned on the circuit breaker and flipped the light switch. The

lamp still didn't work. It turns out that the switch was bad. Like all other engineers, I was curious, so I put the old ballast back in. The light worked perfectly. Now, this story should tell all you troubleshooters to not make assumptions without testing them. A minute with a voltmeter would have shown that the switch was defective.

I will forever cherish this memory because, when the next day I took the new fluorescent ballast back to Orchard Supply Hardware, I was honest with the store manager who was manning the returns counter. I explained that I thought I had a bad ballast but that the problem had turned out to be the switch. I then showed him where the wire nuts had grooved the wires on the ballast and told him I would understand if they wouldn't let me return it. "Of course we'll take it back," he responded. "The important thing is that you got your light fixed." I have been a loyal customer at Orchard Supply ever since. I don't care if I can get something cheaper at a big-box store. Orchard Supply gets my business.

More recently, I saw both sides of the customer-service coin. A friend had a heart attack and needed a char-



**Businesses are here for the customers, not the other way around.**

ger for his cell phone in the hospital room. I guess he was too embarrassed to let me see his apartment. I went to a local Verizon store with the model number. To my amazement, the store had no charger for his two-year-old phone, and the employees had no recommendations about where I could find one. They just didn't care. I might as well have been in a Denny's.

So I went to Micro Center across the mall. After hearing about my friend in the hospital, a store employee browsed through the shelves with me, show-

ing me everything that might work. We agreed I should buy a \$50 universal charger and hope for the best. Unfortunately, the charger didn't fit, but, when I took it back to Micro Center, I found out that it was over the 30-day limit for returns. I started to inundate the return clerk with an avalanche of excuses, adding how carefully I had repacked the box. She stopped me after I showed her the receipt and said, "Oh, this isn't too far out." She scanned the bar code and told me that I would receive the full credit on my credit card—no hassle, no argument, no restocking fee—nothing but a smile and a thank you. I immediately bought some blank-DVD media and cable-routing hardware that cost more than the \$50 credit I had just received.

Just two weeks ago, I was in Portland, OR, visiting an old college buddy. We went to a trendy local supermarket that he said had restaurant-quality steaks. We bought three at \$15 a pound. As we waited to check out, we got a call from his brother-in-law who was having car troubles on the way to visit us and needed our help. We went back to the meat counter and explained the situation, and they cheerfully took the steaks back. When the car problem turned out to be a false alarm, we returned 20 minutes later and bought four steaks.

When times are good, we take our customers for granted. Hunt down *The Suicidal Corporation* to read how corporate narcissism made Ford Motors think it was the customer's *duty* in the 1980s to buy a car every two years (**Reference 1**). There is no need to worry about the downturn if you realize businesses are here for the customers, not the other way around. **EDN**

### REFERENCE

**1** Weaver, Paul H, *The Suicidal Corporation: How Big Business Fails America*, Touchstone Books, 1989, ISBN: 0-671-67559-1.

Contact me at [paul.rako@edn.com](mailto:paul.rako@edn.com).



# EDN

## PRESIDENT, BOSTON DIVISION, REED BUSINESS INFORMATION

Mark Finkelstein, mark.finkelstein@reedbusiness.com  
1-781-734-8431

### PUBLISHER, EDN WORLDWIDE

Russell E Pratt, 1-781-734-8417;  
rpratt@reedbusiness.com

### ASSOCIATE PUBLISHER, EDN WORLDWIDE

Judy Hayes, 1-925-736-7617;  
judy.hayes@reedbusiness.com

### EDITOR-IN-CHIEF, EDN WORLDWIDE

Rick Nelson, 1-781-734-8418;  
rnelson@reedbusiness.com

### EXECUTIVE EDITOR

Ron Wilson, 1-510-744-1263;  
ronald.wilson@reedbusiness.com

### MANAGING EDITOR

Amy Norcross  
1-781-734-8436;  
fax: 1-720-356-9161;  
amy.norcross@reedbusiness.com  
Contact for contributed technical articles

### SENIOR ART DIRECTOR

Mike O'Leary  
1-781-734-8307;  
fax: 1-303-265-3021;  
moleary@reedbusiness.com

### ANALOG

Paul Rako, Technical Editor  
1-408-745-1994;  
paul.rako@edn.com

### MASS STORAGE, MULTIMEDIA, PCs, AND PERIPHERALS

Brian Dipert, Senior Technical Editor  
1-916-760-0159;  
fax: 1-303-265-3187;  
bdipert@edn.com

### MICROPROCESSORS, DSPs, AND TOOLS

Robert Cravotta, Technical Editor  
1-661-296-5096;  
fax: 1-303-265-3116;  
rcravotta@edn.com

### NEWS

Suzanne Deffree, Managing Editor  
1-631-266-3433;  
sdeffree@reedbusiness.com

### POWER SOURCES, ONLINE INITIATIVES

Margery Conner, Technical Editor  
1-805-461-8242;  
fax: 1-805-461-9640;  
mconner@reedbusiness.com

### DESIGN IDEAS EDITOR

Martin Rowe,  
Senior Technical Editor,  
*Test & Measurement World*  
edndesignideas@reedbusiness.com

### SENIOR ASSOCIATE EDITOR

Frances T Granville  
1-781-734-8439;  
fax: 1-303-265-3131;  
f.granville@reedbusiness.com

### EDITORIAL/WEB PRODUCTION

Diane Malone, Manager  
1-781-734-8445; fax: 1-303-265-3024  
Steve Mahoney,  
Production/Editorial Coordinator  
1-781-734-8442; fax: 1-303-265-3198  
Melissa Annand,

Newsletter/Editorial Coordinator  
1-781-734-8443; fax: 1-303-265-3279  
Adam Odoardi, Prepress Manager  
1-781-734-8325; fax: 1-303-265-3042

### CONSULTING EDITOR

Jim Williams, Staff Scientist,  
Linear Technology

### CONTRIBUTING TECHNICAL EDITORS

Dan Strassberg,  
strassbergedn@att.net  
Nicholas Cravotta,  
editor@nicholascravotta.com

### COLUMNISTS

Howard Johnson, PhD, Signal Consulting  
Bonnie Baker, Texas Instruments  
Pallab Chatterjee, SiliconMap

### PRODUCTION

Dorothy Buchholz,  
Group Production Director  
1-781-734-8329  
Joshua S Levin-Epstein,  
Production Manager  
1-781-734-8333; fax: 1-781-734-8096

### EDN EUROPE

Graham Prophet, Editor, Reed Publishing  
The Quadrant, Sutton, Surrey SM2 5AS  
+44 118 935 1650;  
fax: +44 118 935 1670;  
gprophet@reedbusiness.com

### EDN ASIA

Luke Rattigan, Chief Executive Officer  
luke.rattigan@rbi-asia.com  
Kirtimaya Varma, Editor-in-Chief  
kirti.varma@rbi-asia.com

### EDN CHINA

William Zhang,  
Publisher and Editorial Director  
wmzhang@idg-rbi.com.cn  
Jeff Lu, Executive Editor  
jefflu@rbichina.com.cn

### EDN JAPAN

Katsuya Watanabe, Publisher  
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34410A	6 1/2	0.0030%	10,000 / sec	2.6 ms	GPIO, USB, LAN (LXI)
34411A/ L4411A	6 1/2	0.0030%	50,000 / sec	2.6 ms	GPIO, USB, LAN (LXI)
34420A	7 1/2	0.0030%	250 / sec	.02 sec	GPIO, RS-232
3458A	8 1/2	0.0008%	100,000 / sec	3.0 ms	GPIO

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# pulse

INNOVATIONS & INNOVATORS

## Hard-disk drive touts 2-Tbyte storage, speedier spins

Last month, I believed that Western Digital ([www.wdc.com](http://www.wdc.com)) was still the only vendor manufacturing 2-Tbyte, 3.5-in. hard-disk drives in high volumes (see "Western Digital packs 1 Tbyte into 2.5-in. disk," *EDN*, Aug 20, 2009, pg 13, [www.edn.com/article/CA6676179](http://www.edn.com/article/CA6676179)). As it turns out, I wasn't exactly right; Seagate ([www.seagate.com](http://www.seagate.com)) recently began selling a 2-Tbyte member of its Barracuda LP family, which the company unveiled in April. Seagate's ST320005N4A1AS-RK, a four-platter, eight-head configuration, spins at 5900 rpm. Western Digital, conversely, doesn't specify a rotation-per-minute performance metric for its four-platter WD20EADS, instead relying on a nebulous "IntelliPower" marketing moniker. The IntelliPower algorithm dynamically varies rotational speed to optimize performance versus power consumption at any time.

As for faster-rotating, 2-Tbyte variants, Seagate is still not shipping its previously announced 7200-rpm drive. Hitachi, with its recently announced \$329 Deskstar 7K2000, is the first to reach that vaunted threshold. Whereas the competing drives are four-platter models—that is, 500 Gbytes/platter—the Deskstar 7K2000 is a five-platter, 400-Gbyte/platter, 10-head configuration. Hitachi squeezed this abundance of magnetic media into the 3.5-in. form factor's standard 1.028-in. (26.1-mm) height. However, as with Hitachi's four-platter, 1-Tbyte hard-disk drive that it unveiled in early 2007, you should expect the Deskstar 7K2000 to on average burn more power than a future equivalent with fewer platters, with all other specs being equal.

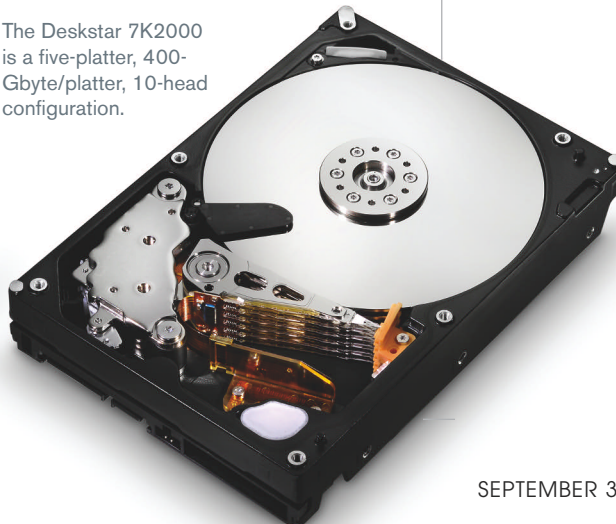
What's with the platter-count discrepancy between manufacturers? Think about it: As a

platter spins ever faster, it becomes increasingly challenging for the read/write head to discriminate between sequentially stored data bits. That difficulty is fundamentally the reason that Hitachi's 7200-rpm drive needs five platters to deliver the same aggregate capacity as Western Digital's and Seagate's slower-spinning four-platter competitors.

PMR (perpendicular-magnetic-recording) technology and other techniques over time enable disk-drive suppliers to squeeze ever-increasing bit counts onto a given-sized sliver of magnetic media. The same press release that launches the Deskstar 7K2000 provides a hint about where Hitachi will shortly be going, stating that, in addition to the new drive, Hitachi is refreshing its high-volume desktop-hard-drive family. The new 7200-rpm Deskstar 7K1000.C family will deliver as much as 500 Gbytes per platter and will come in capacities of 160 Gbytes to 1 Tbyte. Volume production of the new Deskstar 7K1000.C will begin this quarter.—by Brian Dipert

▶ **Hitachi**, [www.hitachi.com](http://www.hitachi.com).

The Deskstar 7K2000 is a five-platter, 400-Gbyte/platter, 10-head configuration.



### FEEDBACK LOOP

**“Sometimes, it is just not worthwhile to ‘play the game’ with some companies. Here is another question: Do we ... really need that standard?”**

—Electrical engineer William Ketel, in *EDN*'s Feedback Loop, at [www.edn.com/article/CA6674036](http://www.edn.com/article/CA6674036). Add your comments.

## Solder-in scope probes reduce rise times, ac loading, and probe noise

LeCroy's line of WaveLink high-bandwidth differential solder-in probes provides rise-time performance of 20 psec for a 20-GHz probe with a 20-GHz oscilloscope. This figure is the same rise time as that of the scope alone. Probe noise is 25 nV rms/ $\sqrt{\text{Hz}}$  and minimum high-frequency ac loading is 175 $\Omega$ . According to the manufacturer, these probes' signal fidelity, which is essential for accurately characterizing next-generation serial data, more closely approximates that of cabled inputs than does that of any similar-bandwidth probes.

Like the lower-bandwidth WaveLink probes, the high-bandwidth WaveLink probes use a transmission-line design with an attenuating tip followed by an amplifier whose output drives a differential-transmission line, which connects to the scope through a platform/cable assembly. LeCroy pioneered this architecture, which provides superior performance at high bandwidth and is now the standard for probes whose bandwidth exceeds 6 GHz.

The new series includes three amplifier/tip modules: the \$7990, 13-GHz D1305; the \$10,990, 16-GHz D1605; and

the \$14,990, 20-GHz D2005. Each includes an amplifier of the rated bandwidth, two solder-in tips, 10 spare damping resistors, and a variety of clips and clamps to hold the solder-in tip or amplifier and prevent movement. In addition, the series includes two models of platform/cable assemblies: the WL-PLink-A and the WL-2.92MM. Each includes a mounting clamp, a probe holder, and a deskew fixture.

The WL-PLink-A connects to the ProLink probe inputs, which all of the manufacturer's WaveMaster 8 Zi scopes use for inputs at frequencies as high as 16 GHz and the SDA18000 serial-data-analyzer instruments use at frequencies as high as 18 GHz. The WL-2.92MM connects to the 2.92-mm inputs of the 20-GHz WM 820Zi, 25-GHz 825Zi, and 30-GHz 830Zi scopes. This probe architecture enables you to use a single amplifier/tip module with either the ProLink or the 92-mm inputs of WM 8 Zi ultrahigh-bandwidth scopes. Because the amplifier/tip assembly represents a large percentage of a high-bandwidth probe's cost, this flexibility provides a significant advantage.

To achieve superior broadband performance, the new

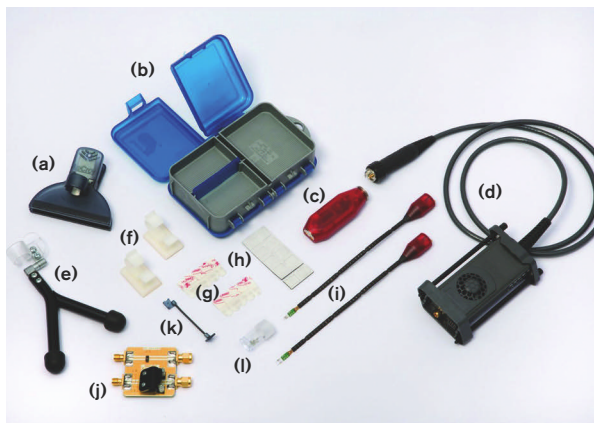
probes incorporate an advanced differential traveling-wave (distributed) amplifier, which maximizes gain per stage, limits probe attenuation to 2.5 times, and provides 25-nV-rms/ $\sqrt{\text{Hz}}$  probe noise, yielding rms noise of 2.9 mV at 13 GHz, 3.2 mV at 16 GHz, and 3.5 mV at 20 GHz. This amplifier also provides ample bandwidth to minimize rise times displayed on WM 8 Zi scopes of equivalent bandwidth. The rise-time specification of the probe/scope combination is the same as that of the scope itself, permitting use of a probe for critical measurements without increasing the displayed waveforms' rise time. This characteristic is especially important when you must conserve scope channels to allow multiple differential-signal measurements when you work on multilane buses, for example.

The 16- and 20-GHz probes' minimum high-frequency ac loading is much lower than that of competitive units; the 13-GHz probe's minimum loading is roughly equal to that of competitive units. These attributes enable the WaveLink probes to provide high signal fidelity and accurately reproduce signals without drawing excessive current, which can affect the circuit under test and invalidate the measurement.

LeCroy has also improved its popular solder-in-tip design by making the tip's damping resistors field-replaceable. If you damage a tip, you can simply solder in a new resistor and quickly resume work. Each solder-in probe comes with 10 spare damping resistors, and you can order more.

—by Dan Strassberg

► LeCroy Corp, [www.lecroy.com](http://www.lecroy.com).



The WaveLink high-bandwidth differential solder-in scope-probe system comprises a platform clamp (a), a plastic storage case (b), an amplifier (c), a platform/cable assembly (probe body, d), the FreeHand probe holder (e), adhesive-backed tip-retaining clips (f), an adhesive-pad kit (g and h), a solder-in tip (i), a deskew fixture (j), a tip-retaining clip (k), and spare damping resistors (l).

### DILBERT By Scott Adams



# Tanner EDA announces router, layout-device generator

At the Design Automation Conference ([www.dac.com](http://www.dac.com)), which took place in July in San Francisco, Tanner EDA introduced the SDL (schematic-driven-layout) interactive autorouter and the DevGen layout-device generator. The company also announced that it is shipping Version 14.10 of its Tanner Tools Pro and HiPer Silicon products, which serve full-custom analog and MEMS (microelectromechanical-system) design.

Tanner EDA's SDL software integrates the new SDL Router automatic-routing engine. It speeds layout by automatically routing noncritical nets and allowing designers to focus on routes that require expensive handcrafting to achieve performance or to address analog-sensitive nets or parts of nets. A layout engineer interactively controls the router, which natively employs user-created routing geometry; it runs on all or a specified subset of nodes on each pass. Users can manually route part of a net and

have the router automatically finish routing the net. Users can highlight and rip up nodes, manage the manual and automatic routing status, and implement engineering change orders.

Using DevGen along with SDL allows analog-layout designers to become more productive by automating much of the tedious task of laying out devices. DevGen provides parameterized layout generators that are configurable for any process. By using the DevGen wizard and answering a few questions about the layers involved and the DRCs (design-rule checks), designers can create parameterized cells of common devices without writing code. DevGen includes layout generators for capacitors, resistors, inductors, MOSFETs, and diodes.

SDL Router and DevGen maintain close synchronization between the schematic and the layout. SDL automates instantiating of cells and parameterized devices and placement

quality by displaying real-time node fly lines. It also helps avoid routing congestion and tracks an engineer's progress to help manage workflow.

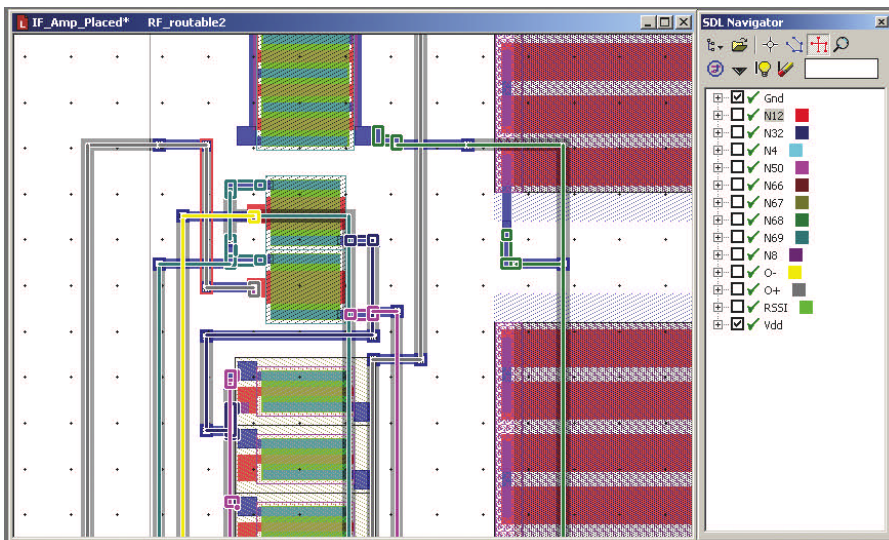
Besides the new SDL Router and DevGen, Version 14.10 of Tanner Tools Pro and HiPer Silicon include improved Verilog-A integration, which reduces analog-simulation runtime when simulations include digital blocks, and HiPer Verify, which natively runs Calibre, Dracula, and Assura foundry files without conversion or modification. The tools perform SOA (safe-operating-area) checks in T-Spice, so models stay valid and circuits operate correctly. Interactive DRC displays violations in real time during layout editing. The software displays the spacing distance in real time while the designer edits the layout and can prevent editing from getting closer than the minimum distance. Prices for the packages start at \$25,000.—by Rick Nelson

► **Tanner EDA**, [www.tannereda.com](http://www.tannereda.com).

## CHOPPER OP AMP DRAWS 17- $\mu$ A POWER-SUPPLY CURRENT

Analog Devices has announced the **ADA4051-2** dual operational amplifier that has 2- $\mu$ V typical offset and 15- $\mu$ V maximum offset. The part operates at 1.8 to 5.5V and draws a maximum of 17- $\mu$ A power-supply current. It achieves a **PSSR** (power-supply-rejection ratio) and a **CMRR** (common-mode-rejection ratio) of 135 dB and has a gain-bandwidth product of 125 kHz and a dynamic range greater than 110 dB. Temperature drift is less than 20 nV/ $^{\circ}$ C. The device's input and output operate from rail to rail.

The **ADA4051-2** dual op amp in an eight-pin **LFSCP** operates at -40 to +125 $^{\circ}$ C, and the 3 $\times$ 3-mm, eight-pin **MSOP** version operates at -40 to +150 $^{\circ}$ C. Each device costs \$1.50 (1000).—by Paul Rako  
► **Analog Devices**, [www.analog.com](http://www.analog.com).



The SDL Router automatic-routing engine is part of Tanner EDA's SDL software.



The low-offset, zero-drift ADA4051-2 amplifier finds use in portable and battery-powered instruments requiring high dc precision and measurement stability, such as gas analyzers, remote sensors, handheld medical devices, and consumer-gaming controllers.



**RESEARCH UPDATE**

BY RON WILSON

## DSP brings you a high-definition moon walk

The National Aeronautics and Space Administration ([www.nasa.gov](http://www.nasa.gov)) recently discovered that someone at the agency recorded over the master copy of the video of Neil Armstrong's famous Apollo 11 walk on the moon. One small step for one man succumbed to one major error by another. Surviving, however, are myriad transcoded copies, edited versions, and

other variants on the original recording. None has the information content of the original 1-in. master tape, which NASA says has been degaussed, re-certified, and reused—no doubt for something more historic.

Nonetheless, John Lowry, founder of Lowry Digital, reasoned that the video might hold enough information to re-create the original recording and

Lowry Digital has started to recover the lost Apollo 11 video, thanks to some difficult digital image processing.

maybe even to interpolate it to high definition. Lowry's company has developed the necessary image-enhancement technology, having initially developed it for use on later Apollo missions. This new project slightly differs, however. This time, Lowry is working primarily from four sources with assistance from a variety of other recordings. Apollo 11 transmitted the original video back to Earth on a 10-frame/sec, 320-line, slow-scan downlink. A number of recordings exist in which scientists have rescanned and frame-shifted this source into PAL (phase-alternating-line) or NTSC (National Television System Committee) formats. One other source that is the only option for some of the material is a film from a spring-driven, 8-mm, 16-frame/sec movie camera that someone at Mission Control

aimed at a TV monitor during the mission.

The restoration will primarily use Lowry Digital's temporal image processing, which processes long sequences of frames to remove transient noise. Scientists at the company have also added corrections for problems specific to this material, including vignetting, limited dynamic range and ghosting in the imaging tube in the original RCA camera, time distortions during format conversions, and noise from media aging.

Lowry is reportedly using Nvidia ([www.nvidia.com](http://www.nvidia.com)) Tesla GPUs (graphics-processing units) programmed in the company's CUDA (Compute Unified Device Architecture) to implement the algorithms. Nvidia claims that the GPUs are approximately two orders of magnitude faster than CPU computations, reducing the processing time to less than one minute per frame.

► **Lowry Digital**, [www.lowrydigital.com](http://www.lowrydigital.com).

## MASKLESS COPPER DEPOSITION COULD SLASH METALLIZATION COSTS IN ICs

Whereas much rocket science goes into making the minimum-geometry metal lines at the bottom of the interconnect stack on an IC, no one pays much attention to making the upper metal layers on which the spacing is relaxed, the metal is thick, and some processes still use aluminum. A relatively new idea from Replisaurus could address those problems.

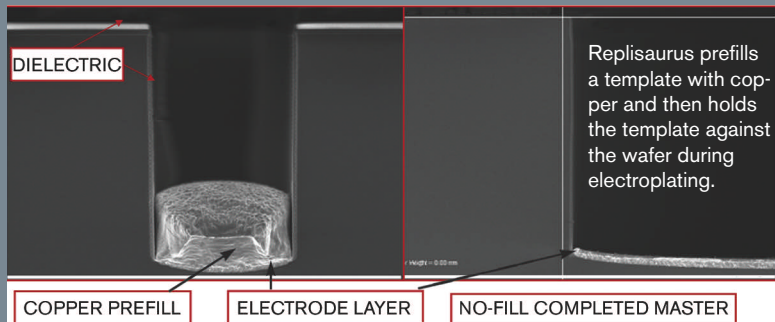
Replisaurus makes an oxide-on-wafer template, etching it so that a trench is everywhere in the oxide that requires copper on your IC wafer. The company then coats the bottom of each trench with a reusable electrode material. This step makes each trench in the template into a micro-sized electroplating chamber, with the template oxide forming the top

and sidewalls and the target wafer forming the base.

To use the template, you deposit approximately 5 microns of copper into the trenches. You then press the template onto the surface of a wafer, which you have prepared with a copper-seed layer. When you turn on the power, the copper in the trenches electroplates onto the seed layer of

the IC wafer. Each trench contains its electroplating process, so you get an accurate shape and controllable thickness of copper on the wafer. After plating, you strip any remaining copper from the template. You get about 500 prints from a template before it wears out.

► **Replisaurus Technologies**, [www.replisaurus.com](http://www.replisaurus.com).



09.03.09

# 1-Wire<sup>®</sup> ADVANTAGE

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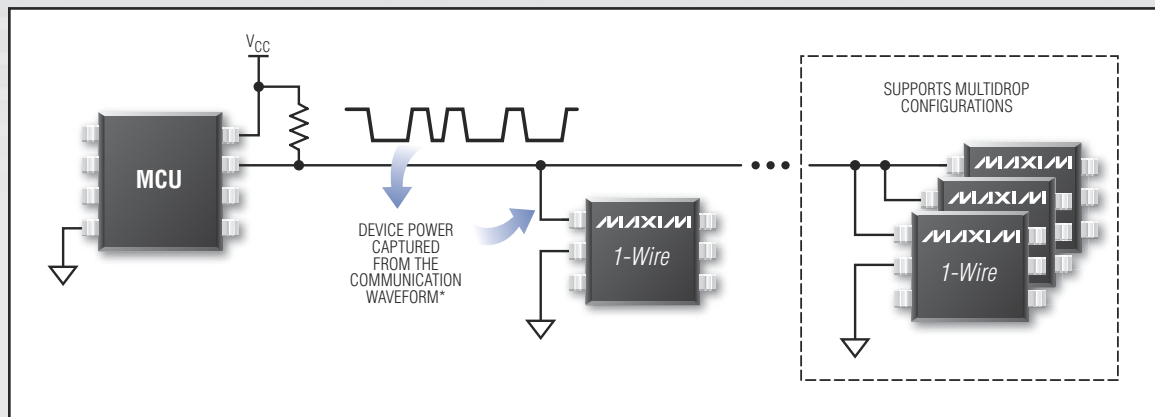


## Customer's Concern

Needs to add or control electronic functionality over a pin-limited connector or processor interface, potentially with a strong ESD performance requirement.

## Maxim's Solution

1-Wire devices enable designers to add memory, security, control, and other mixed-signal functions over a single contact, easily and efficiently. ESD performance typically exceeds  $\pm 8\text{kV}$  Human Body Model.



## How It Works

The 1-Wire bus is a simple signaling scheme that performs serial communication between a host/master controller and one or more 1-Wire slaves sharing a common data line. Both power and data communication for slave devices are transmitted over the single-contact 1-Wire line.

## Optimized for Your Application's Requirements

- Unique, Factory-Programmed, Electronic Serial Numbers for Tracking or Security Functions
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- Crypto-Strong Authentication Enables
  - License Management
  - Protection Against NV Data Modification
  - Bidirectional Host-Peripheral Authentication, Possibly over a Network
  - Clone Prevention
- Single or Multipoint Temperature Sensing with Minimal Wiring Complexity/Cost
- I/O Sensing and Control
- Operation over Pin-Limited Connectors or with I/O-Limited MCU

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

\*1-Wire devices with special features may require an additional power source.

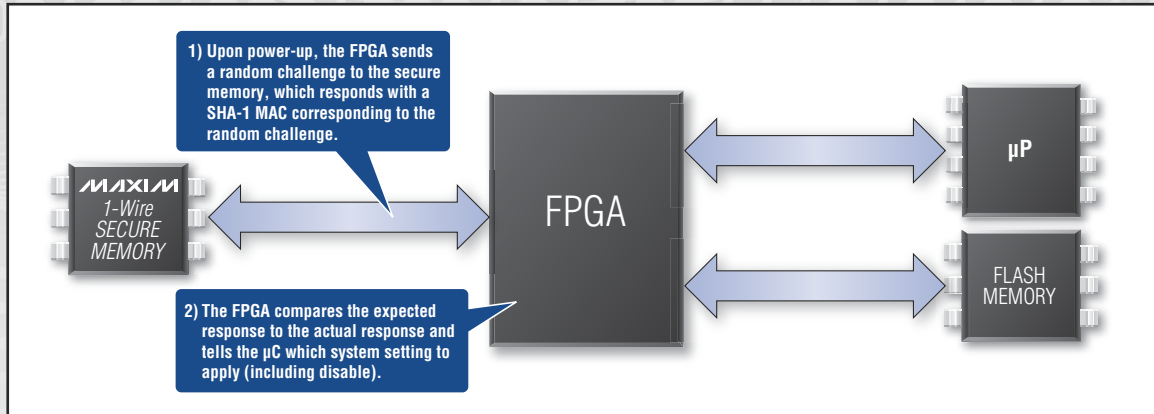
**MAXIM**  
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## Customer's Concern

Need to securely and cost-effectively protect an FPGA design against unauthorized copying.

## Maxim's Solution

Crypto-strong 1-Wire secure memories provide the FPGA design with a proven mechanism to self-test for validity.



## How It Works

1-Wire memories utilize a FIPS 180-3 (ISO/IEC 10118-3) Secure Hash Algorithm (SHA-1) to implement a challenge-and-response authentication solution based on a private key. The success or failure of the FPGA authentication sequence is used by the system to set operation or action.

## Reference Designs

Easy-to-use reference designs utilizing this cost-optimized copy protection scheme are available by the leading FPGA manufacturers. Visit [www.maxim-ic.com/fpga](http://www.maxim-ic.com/fpga) for more information.

## A Sampling of Innovative 1-Wire Solutions

1-Wire Product Family Function	Customer-Favorite Maxim Device
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EEPROM	DS2431: 1Kb EEPROM
Crypto-secure authentication	DS28E01-100: SHA-1 authenticated EEPROM
<b>Additional 1-Wire Devices</b>	
Temperature measurement	DS28EA00: $\pm 0.5^{\circ}\text{C}$ accurate digital temp sensor
OTP EPROM	DS2502: 1Kb EPROM
General-purpose I/O	DS2413: 2-channel switch with 28V/20mA GPIO
Unique, 64-bit serial number	DS2401: 64-bit ROM serial number
Real-time clock	DS2417: 32-bit RTC counter

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BY HOWARD JOHNSON, PhD

## Sliding edge

**W**hen you connect 50Ω traces on two boards made from dissimilar fiberglass-laminate materials, will high-speed signals reflect due to the sudden change in board properties as they move across the connection interface? This question arises because, in most cases, the boards have different transmission-line geometries. For example, comparing two PCBs (printed-circuit boards) having the same layer thickness, one with a dielectric constant of 4.3 and the

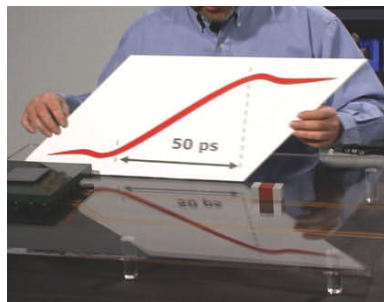
other with a dielectric constant of 3.5, the second board must use wider traces to obtain the same 50Ω characteristic impedance as the first. The adjustment of trace width and height to accommodate dielectric materials is a normal part of PCB manufacturing.

At the point of connection, assuming a perfect butt joint between the boards with no intervening connector, the abrupt change in trace width throws the local per-unit-length values of inductance and capacitance into chaos. That scenario sounds terrible, but, fortunately, the disruption persists only a short distance on either side of the joint. If you move a couple of trace heights away from the joint in either direction, each board exhibits its designed value of 50Ω. Your signal does not care about the impedance at any one spot. It cares only about the effective average characteristic impedance under each signal edge as it moves through the transmission structure.

The “telegrapher’s model” of a transmission line employs a similar averaging principle. That model comprises a cascaded ladder filter with discrete blocks, each having one series inductor and one shunt capacitor. As long as the delay of each block remains short-

er than the signal’s rise or fall time, the signal propagates through the circuit as if it were a continuous transmission pathway. The local impedance, if you could define such a thing, radically alternates from purely inductive to purely capacitive as your signal moves along. This fact causes no great difficulties as long as the average ratio of inductance to capacitance remains fixed. The number of blocks a signal edge spans as it moves through the structure represents in some sense the “length” of the edge.

Each signal edge in a PCB trace has a definite physical length equal to the rise or fall time in seconds times



**Figure 1** A 50-psec edge emanating from a BGA package slides down a transmission line.

its propagation velocity in meters per second. In British units, the way most engineers still design PCBs, the propagation delay of 4.3 works out to roughly 6 in./nsec. If the signal-edge transition time is 50 psec, then the physical length of that edge is 0.3 in.: (0.050 nsec)(6 in./nsec). If your typical PCB’s trace height is 5 mils, then a 50-psec rising edge, spanning a length of 300 mils, looms much larger than the disruption zone.

Imagine a 50-psec signal edge sliding along the first PCB trace (**Figure 1**). Slide it halfway onto the next board. Now, freeze time. Consider the value of the average impedance under a signal edge as it sits straddling the interface. To the left of the joint, as you look deep into the first PCB, the impedance appears correct. Near the joint, an abrupt change in trace width may disrupt the local impedance. Looking farther to the right, you can see that the impedance returns to its designed value of 50Ω. If the signal edge spans a length much greater than the size of the disrupted zone, the averaging process cancels out the effects of the disruption with long sections of unmolested 50Ω transmission on either side of the joint. In that case, the disruption causes no difficulties. You run into trouble only when you reach such high speeds that the physical length of your signal edge shrinks to a size comparable with the impedance disruption.

These observations apply only to situations in which the characteristic impedance remains the same on both sides of the interface. **EDN**

*Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at [www.sigcon.com](http://www.sigcon.com) or e-mail him at [howie03@sigcon.com](mailto:howie03@sigcon.com).*

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IN THIS CLIMATE, OUTSOURCING IS BECOMING A MANDATORY SKILL FOR IC-DESIGN MANAGERS. BUT IT'S NOT INTUITIVELY OBVIOUS.

# OUTSOURCING AN IC DESIGN: SOME ADVICE FROM THE TRENCHES

BY RON WILSON • EXECUTIVE EDITOR

**T**here are many reasons to consider outsourcing all or part of a chip design. Perhaps you are on a board-level-design team, and the correct approach to your new project is a chip that doesn't today exist. Perhaps your team has previously done IC designs but lacks the skills for your next project. Maybe your organization has downsized so that only a few key individuals remain from what was once a full SOC (system-on-chip)-design team. In each of these cases, outsourcing may be the answer. In every case, however, defining the work, selecting the right vendor, and creating an adequate project-management structure are necessary conditions for success.

It's not easy to learn from others' experiences in outsourcing. Some companies—particularly in the fables area—don't want to admit that they use outsource vendors. Others don't discuss the question out of concern that revealing

their vendors or their management approaches might somehow give away a competitive advantage. A few experienced design teams and a few vendors share their ideas about what they've learned on the subject.

Reasons to outsource all or part of a chip design come down to two points: expertise and profit. And these two are themselves interrelated. "There are two categories of reasons people call us," says Jack Harding, chairman, president, and chief executive officer of eSilicon. "Customers do initiate the contact about two-thirds of the time. There are the reasons the customers tell us, and there are the underlying reasons that we infer."

Customers say that they need an outside vendor to help balance the load on their engineering team, that they want to avoid the cost of retooling, or that, because of eSilicon's volumes, it can negotiate a better deal than they can on IP (intellectual-property) licenses or wafers, Harding explains. "These things may be true," he says, "but the underlying issue is often that the number of design starts a team does in a year has

declined until it's become hard for the internal people to stay current with the tools." Meanwhile, the number of skills the team needs to succeed on a design keeps increasing. At some point, the engineering manager has to look at the capital distribution and decide whether to keep a full in-house design team.

This analysis often concludes that a small company should focus its engineering resources on its key differential advantages, rather than pay for the ability to execute a full chip-design flow. QuickLogic, for example, sells CSSP (customer-specific-standard-product) chips (Figure 1) that include both fixed blocks—interface controllers, buffer memories, and so forth—to implement a platform chip and a programmable-logic fabric so that a user can customize the chip for an application. QuickLogic's secret sauce is in the logic fabric rather than cell-based SOC design. Accordingly, the company outsources the fixed-function design and chip integration to a contractor and keeps chip architecture and the programmable-logic array with its proprietary antifuse technology in-house.

Similarly, RF signal-processing vendor Scintera Networks sees chip architecture and analog/mixed-signal design as its key areas of expertise. "We do about one digital design per year," says Bob Koupal, vice president of engineering at the company. "So we don't use the digital tool chain that much. It doesn't make sense for us to staff and tool up for a digital back-end flow." Instead, Scintera turned to Fastrack Design and Axi-

**AT A GLANCE**

- ▣ Outsourcing can take many forms in a chip design.
- ▣ Selecting a vendor is both a technical and a personal decision.
- ▣ Any outsource work requires close management.
- ▣ Many companies have seen the last of full in-house chip-design teams.

om Design Automation to provide synthesis through back-end design and to perform verification on the digital portions of a recent design, respectively.

### PREPARATIONS

Experienced outsourcers emphasize that it is vital to go into the engagement with a detailed understanding of the skills you will require from your vendor. "We defined three criteria for our vendor search," says Ajith Dasari, QuickLogic's vice president of engineering. "First, we looked for a specific level of technical capability. Second, we looked for scalability. Could the vendor handle not just the first chip, but also the whole platform as it unfolded? Third, we looked at economics. Is this [approach] really going to be more economical than using the team I have?"

There may be other important criteria, as well. Koupal wanted a vendor whose tool flow would match Scintera's. "In a way, we chose our vendors first for their tool set and then for their capabilities," he says.

Although most outsource relationships follow an ASIC-style pattern—the customer hands off a verified netlist to the contractor—it is possible to outsource any part of the chip or any part of the flow (Figure 2). Alternatively, you can outsource an entire chip design and have only applications—but not chip-design—expertise in-house. If you lack the in-house expertise to evaluate your contractor's work, you may want to outsource this oversight function, as well. Harding says that eSilicon is working on one project in which the company's role is to evaluate a design that another contractor did.

Once you have established the criteria and estimated the scope of the work, it's time to start looking for prospective vendors. In real life, the search is often more informal than exhaustive. Scintera looked first at vendors it had used before. Dasari worked through his personal network to get recommendations for vendors that might fit QuickLogic's project requirements. Often, first- or second-hand experience is the most trusted tool for building a short list. When you have the short list, the detailed investigation starts, and this inquiry quickly moves from the technical to the personal.

"Before we made a final decision, we asked the vendors to actually send the key people we'd be working with to our office," Koupal says. "The engineers came from India, and we interviewed them here. It sounds like a lot to ask, but the vendors understood why we needed to [take this approach]."

These interviews can become intense. "We kept asking questions in increasing detail until we felt we understood how much the guys really knew," Dasari says. "For instance, we would define a block and then ask them for estimates on final power and timing. Checking their estimates against our experience told us about how much work they'd done with our kinds of structures."

### GETTING DOWN TO WORK

Once you've chosen a vendor, it's time to get to work. Often, the first step is to distill a general understanding of the project into a detailed statement of work. This document may figure in price negotiations and become a key project-management tool. Accordingly, it can be quite detailed. The statement

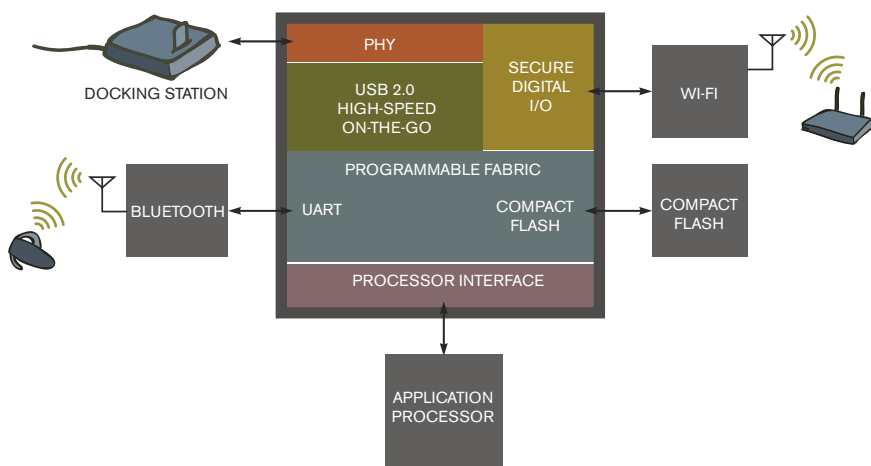


Figure 1 QuickLogic's CSSPs combine fixed-function interfaces with programmable-logic fabric.

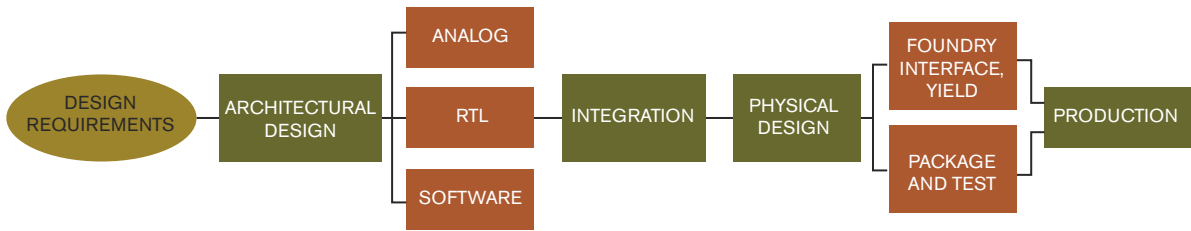


Figure 2 An SOC design comprises many steps, of which a design team may outsource all but the first.

of work may contain architectural descriptions; requirements for function, area, speed, and power on individual blocks; detailed itemization of the flow the vendor will use; completion criteria for each stage in the design and verification tasks; and a schedule. It is not wise to hurry through the statement of work as if it were a formality, experienced managers warn. It's not a pro forma document, but a road map of the joint development. "We spent three or four weeks just developing a document that described the microarchitecture," Dasari says. Koupal, particularly concerned about the interface between his team's analog blocks and the outsourced digital blocks, defined not only the pins in the interface, but also the pins on all the digital blocks.

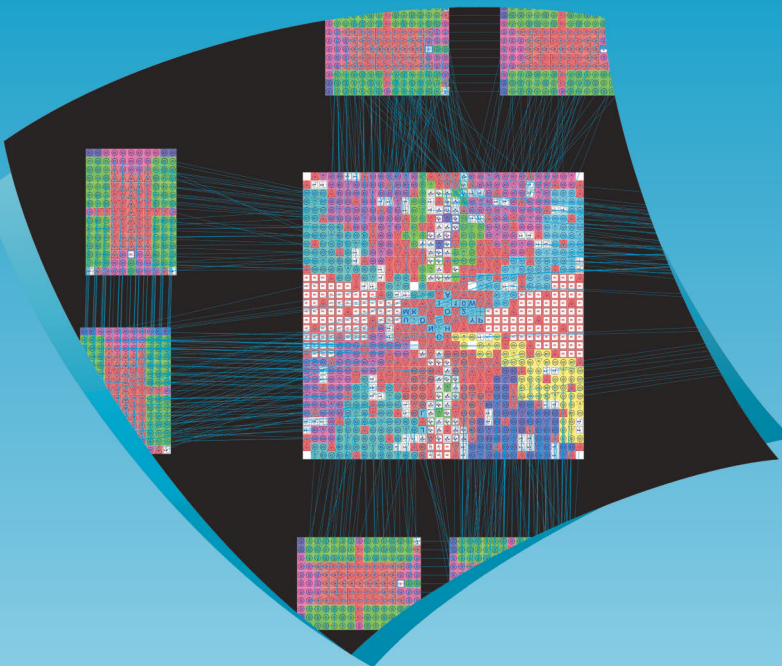
In some cases, though, a shared understanding of the design may be more important than a detailed statement of work. Harding says that, when a new client works with eSilicon for the first time, the client usually shows up with a detailed state-

ment of work. As teams get more experience working with the company, however, the relationship begins to look less like contracting and more like a joint development. Only experience with a team can teach the best trade-off between upfront detail and downstream flexibility.

In addition to the statement of work, managers emphasize the importance of a defined project-management protocol. With or without formal tracking tools, a regimen of closely spaced milestones, regular design reviews, and periodic face-to-face encounters appears essential to keeping the project on track.

Both Koupal and Dasari argue for starting the project with the vendor's senior engineers on-site. The outsource vendor's presence in the building shortens the feedback loop at this early stage when there are lots of questions flowing back and forth between the two teams. It also puts faces on people who would otherwise just be e-mail addresses or voices on the con-

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ference phone during most of the project. There's a more subtle benefit, as well. "Having their senior people start out in our shop for a couple of weeks brought them closer to the project," Dasari says. "When they went back to India, they became the local experts on the project. They were able to deal with a lot of questions locally that would otherwise have required a phone conference the next morning."

Once the project is under way, it settles into a familiar pattern of regular meetings. "We managed the outsource relationship as if it were part of our own company," Dasari says. Both Scintera and QuickLogic used weekly teleconferences as their basic management tool, whether or not the vendor offered any Web-based tracking. "We generated detailed milestones, never more than two weeks apart," Dasari explains. "Then we broke the milestones down into activities, which we tracked in the meetings. At the first hint that someone was struggling with an activity, we could fly our 'tiger team' out there to work with them." That sort of subtle perception would never come through on an activity-tracking report.

This need to understand the nuance of what engineers say in a teleconference is an important issue. The local management team needs to have enough expertise—and strong enough listening skills—to detect whether the project leader in India is saying that the company will be late on closing timing on the DSP datapath or that there's no way it can meet timing requirements and is just spinning its wheels.

That perception requires expertise. Koupal points to his analog/mixed-signal expert and chip architect as indispensable to a successful outcome. Dasari agrees. "You have to have a tiger team. We need one really good guy each in RTL [register-transfer-level] design and physical design to act as project supervisors. You must have your most senior people to successfully manage an outsourced project."

Koupal puts it succinctly. "For us, design outsourcing is a way to amplify the expertise of your in-house people. It's not about doing a project completely outside your range of expertise."

You hope that everything comes together at the end of the project. Again,

⊕ Go to [www.edn.com/090903df](http://www.edn.com/090903df) for more information on the vendors this article mentions.

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managers say, it is vital to have the key outsource people in your office during the final days or weeks of the project to shorten the loop during the frantic scrambles to achieve tapeout.

### MULTIPLE PARTIES

Creating a chip isn't just a two-party affair. Both third-party-IP vendors and at least one foundry will also usually be involved. Multiple outsource vendors may do different parts of the work. Koupal feels strongly that it's a good idea to have different shops do the design work and the verification, even though this arrangement complicates the management process. This attitude mirrors one side of a long-running debate in the industry about the wisdom of having a design team do its own verification. In any case, though, it's important to understand from the outset who will be doing the verification and who will be managing it. Few figures in a chip design are more elusive than verification-coverage metrics, and few more difficult decisions exist than when verification has gone far enough.

Third-party IP presents another complexity. Some outsource vendors differentiate themselves in part on their relationships with a wide range of IP vendors, their ability to get good prices, and their access to timely service. In such cases, Harding says, the outsource vendor would normally take full responsibility for the IP. In other cases, however, the main design team may want to have its own relationships with IP vendors. In this case, according to Dasari, you have to make sure that the license includes provision for your outsource vendor to work with the IP to get it into your chip, and you must be sure that the IP format and deliverables match both the outsource vendor's tool chain and the overall architectural decisions for the chip in such areas as voltages, design-for-test structures, and DFM (design-for-manufacturing) standards.

Foundry relationships can also vary. Companies such as eSilicon not only

maintain foundry relationships, but also own the contracts with the foundry, package, and test houses; own the wafers; and sell packaged silicon directly to their customers. They can develop and qualify second-source foundries, negotiate prices, and manage end-of-life processes, as well.

Sometimes, the foundry relationship goes through the customer, not the outsource vendor. In QuickLogic's case, for instance, the company's programmable logic fabric requires a custom process, so QuickLogic must maintain the foundry relationship. "We pass the PDK [process design kit] to our vendor, and they pass the GDS [graphical-design-system]-II back to us to send to the foundry," Dasari says. Even so, there may be a dotted-line relationship between the foundry and the outsource company anyway, so that PDK updates, process questions, and DFM issues don't find the customer an unwelcome intermediary between the foundry support engineers and the physical design team.

Clearly, no standard technique exists for outsourcing a chip design. You can see a few fundamental principles, however. First, it is vital to have enough in-house expertise to manage the interface between your team and your outsource vendor. Just what this expertise is depends on what you are outsourcing. But you will need this expertise during requirements definition and vendor selection and continuously throughout the management of the design. Second, an outsource relationship requires at least the same level of management as an equivalent in-house design, including a management team that understands the actual state of the project and the objectives, a regimen of frequent detailed reviews, and methods of checks and balances to ensure that every phase of the design is completed correctly. This oversight may require the use of outside resources from a third party.

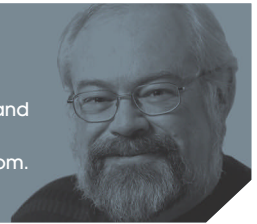
Finally, there is the issue of flexibility. "You do give up some flexibility when you outsource parts of a design," Dasari admits. "You can't just make a big change to the requirements in the middle of the design and expect to have your partner track it. They will see this as a change order, and they'll want to negotiate additional money and schedule, even if the change isn't that big." For some market-

ing-driven organizations, this hurdle may be the largest of all.

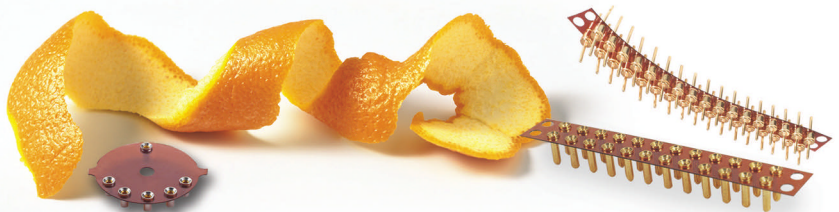
Just as hard economic times are here, design outsourcing is here. For most organizations, it will mean the end of full in-house design teams in favor of small engineering departments that focus on the company's differentiating technology. It also means that a category of professional engineering managers will emerge

who can work with the unique challenge of this organizational structure. **EDN**

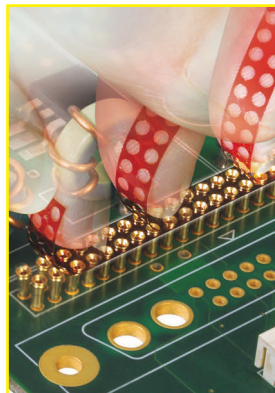
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**Y**ou use galvanic isolation to separate functional sections of electric systems so that charge-carrying particles cannot move from one section to another—that is, no electric current can flow directly from one section to the next. The sections of the system can still exchange energy and information, however, using capacitance, induction, or electromagnetic waves, as well as optical, acoustic, or mechanical means. The technique finds use in situations in which two or more electric circuits must communicate, but their grounds may be at different potentials. It is an effective method of breaking ground loops by preventing unwanted current from traveling between two units sharing a ground conductor. You also use galvanic isolation for safety considerations, preventing accidental current from reaching ground—a building’s floor, for example, through a person’s body. The word “galvanic,” in fact, means having the effect of an electric shock. Knowledge of isolation and its uses may galvanize you into designing it into all your future systems.

The technique should be an integral part of any design because it prevents ground loops, minimizes noise, and, most important, keeps users safe. A lack of isolation can have disastrous results. For example, Sandy Templeton, director of isolator development and applications at NVE, relates that, on two electrical supplies lacking isolation between them, one supply’s ground currents can raise the potential of ground to 50V, melt the cable between two computers, and cause a fire (see **sidebar** “What is ground, anyway?”).

“You don’t know isolation is there, but it’s everywhere,” says Ahsan Javed, product-marketing manager for isolated products at Silicon Labs. He lists a variety of applications requiring isolation, including power supplies, lighting, defibrillators, and hybrid-electric vehicles. Yet, Javed believes that car buyers, for example, are more interested in miles-per-gallon figures or fancy chassis than whether the electrical components integrate isolation. “The end user is ambiva-

YOU MUST DESIGN ISOLATION INTO YOUR CIRCUITS IF YOU WANT TO ENSURE USER SAFETY, ELIMINATE GROUND LOOPS, AND REDUCE NOISE. BEFORE SELECTING A TECHNOLOGY, MAKE SURE THAT YOU UNDERSTAND ALL THE SPECS AND DESIGN CONSIDERATIONS.

BY PAUL RAKO • TECHNICAL EDITOR

# DRAW

## ISOLATION SHIELDS SYSTEMS FROM SHOCKING SURPRISES

# THE LINE



lent to it because it is a safety component,” he says. “You don’t care about your air bag until you need it.”

In another application, medical electronics, it is imperative that you design your systems in such a way that no high voltage from the wall socket or power system can reach—and perhaps kill—the patient. Fortunately, US products must meet the strict certification guidelines of the FDA (Food and Drug Administration). UL (Underwriters Laboratories) also reviews product designs in conferring UL listings (see sidebar “Isolation glossary” in the Web version of this article at [www.edn.com/090903cs](http://www.edn.com/090903cs)).

In a less dramatic application, isolation also filters out noise in electrical systems due to analog and digital grounds and circulating currents (Reference 1). “Galvanic isolation can allow data to pass across two completely isolative ground references,” says David Krakauer, product-line manager of iCoupler products at Analog Devices. Consultant Henry Ott advises careful part place-

### AT A GLANCE

- You use isolation for safety, to eliminate ground loops, or to reduce noise.
- You can replace older analog isolation designs with digital isolators.
- Parts are available to isolate your USB (Universal Serial Bus), RS-232, or I<sup>2</sup>C (inter-integrated-circuit) interface.
- Devices can use optical, RF, capacitive, transformer, and GMR (giant-magneto-resistive) isolation.
- Understand all the specs and design considerations before you select a part.
- Be sure to test your circuitry for every conceivable eventuality.

ment and a disciplined routing strategy on the traces to prevent noise from one part of your circuitry from polluting signals in another part. Sometimes, however, you simply can’t obtain the place-

ment you want. In these cases, Ott advises, use circuit-isolation techniques to ensure that noise from the outside world or other parts of the circuit cannot ruin the signals in your design. Poor ground-plane design can also cause noise. If your isolator allows you to cut up the ground plane in your system and you then run fast digital signals across that cut, the return currents for those signals must now seek the long way around the cut (Figure 1). This scenario is sure to cause EMI (electromagnetic-interference) problems (Reference 2).

When considering techniques for isolating signals, examine the difference between using an isolator as a linear part and as a digital component. When using an isolator in linear mode, you bring an analog signal level across an isolation boundary. When using it in digital mode, you simply bring a high or a low signal across the isolation boundary. You can bring an analog signal across the isolation boundary with discrete parts or by using isolation amplifiers. Alterna-

## WHAT IS GROUND, ANYWAY?

In the 1980s, James McLaughlin was an electronics professor at GMI (General Motors Institute)—now Kettering University. Many of the practical circuit examples he used were for automobiles. He was brutally strict in one area: the definition of “ground.” “If you draw a schematic for a piece of electronics in a car and use the earth-ground symbol, I will fail you for the entire semester,” he said. He explained that the earth-ground symbol (Figure A) represents a 10-foot-high copper-clad steel bar driven into the earth. Water lines or metal gas pipes also constitute earth grounds.

Once you connect a cable, even a braided cable that operates at high frequencies, to earth ground, you add resistance and inductance to the ground-return path. That earth ground is wired to the neutral of your house wiring at the breaker panel and also connects the third-prong ground in duplex outlets. You can reasonably use the earth-ground

symbol for that pin but not for the neutral line because the line contains current. Similarly, if your product plugs into the wall, your schematic should use the earth-ground symbol to indicate the third-prong circuit. Underwriters Laboratories and other safety agencies require that you connect the earth-ground pin of an input connector with a screw or rivet to the metal chassis of a product. On your schematic, then, that connection is the point at which you draw both earth ground and chassis common next to one another and connected.

You might think that the



**Figure A** You should ensure the proper use of earth ground (a), chassis common (b), and signal common (c) for the grounds in your system.

chassis is earth ground, but it is bad practice to use earth-ground symbols for chassis common. You could use the chassis common wherever a power supply or circuit card connects to the chassis. You could show the chassis symbol on a PCB (printed-circuit-board) schematic, but only when a stand-off screws the PCB to the chassis.

Signal-ground symbols are more suitable for depicting circuitry on a PCB. A design can have several of these symbols, with notations to identify them. Different ground systems require a net name so that you do not route them together until you want them to join. Some engineers prefer the term “power-supply return” instead of signal ground. Many engineers eschew using the word “ground” for any signal return, preferring to use “signal common.”

This attitude toward the word “ground” bothers Henry Ott, a signal-integrity consultant. He dislikes the term “ground plane”

tively, if you want to bring signals across the boundary as digital representations, you can use one of many digital isolators. A hybrid approach to the analog/digital-architecture decision employs the use of a delta-sigma modulator to turn your analog signal into a digital PWM (pulse-width-modulated) signal. The part sends that signal across the isolation boundary. Once the signal is over the boundary, you can either use the digital signal as is or send it to a lowpass filter and turn it back into an analog signal.

A discrete transformer approach is a traditional way of providing isolation (Reference 3). Transformers can transmit pulse trains to control an H bridge across a 10,000V boundary (Figure 2). For a detailed schematic, go to [www.edn.com/090903cs](http://www.edn.com/090903cs). You make the pulse transformers by passing three single-turn, 18-kV, UL3239-certified, FEP (fluorinated-ethylene-polypropylene)-insulated, isolated wire loops through a to-

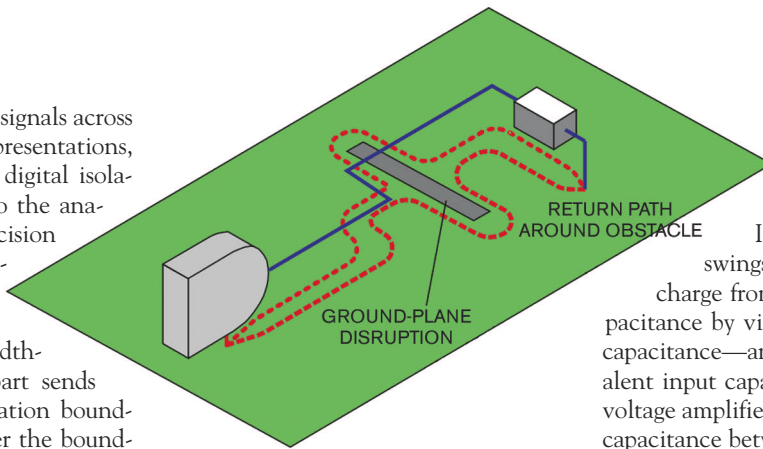


Figure 1 If you run high-speed signals across a slot in a ground plane, you cause the return currents to form a loop and create radiation noise (courtesy Texas Instruments).

roid. It is difficult to find off-the-shelf pulse transformers with 10-kV isolation and UL certification, so you may have to wind your own. A discrete design is also complex, continuously pulsing the FETs with on or off pulses. This approach is preferable, however, to de-

signs that use gate capacitance to maintain the on- or off-state (references 4 and 5).

In those designs, voltage swings on the FET drain push

charge from the gate-to-source capacitance by virtue of the FETs' Miller capacitance—an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance between the input and output terminals. The resulting reduction in gate drive may cause the FET to enter the linear mode and burn up.

Along with discrete designs using transformers, analog optocouplers represent a time-honored—yet tricky—way to bring an accurate analog signal back across an isolation boundary. In optocouplers, the clear plastic inside the part can degrade and get cloudy, and the IR (infrared) LED inside the part can age and produce a lower output. One clever way of surmounting this difficulty is to use a dual optocoupler in your circuit.

because the copper plane in a circuit can't truly be at earth ground, especially at high frequencies. Ott prefers the nomenclature "reference plane" because you reference PCB devices to that potential. "Where is ground on a satellite?" he asks (Reference A). This argument may seem pedantic or overwrought, but proper thinking about ground, common, return, chassis, and reference planes will help you understand the complexities of circuit design. This idea is true of analog circuit design and especially of high-frequency analog circuit design.

One of McLaughlin's co-op students was working at a GM division and had problems getting a car to pass strict Canadian EMI (electromagnetic-interference) standards. The new high-energy ignitions emitted stronger interference, and it seemed that the noise was just sailing past the hood of the car. As any RF engineer would know, the problem was grounding. The division had saved money by putting a little

metal scraper to dig through the paint and "ground" the hood to the car chassis. Knowing that this ground was marginal at best, the engineering team substituted an approximately 12-in.-long, 18-gauge wire. Galvanically connecting the hood of the car to the chassis with a long wire, however, is not really grounding the hood in the RF sense. That 12-in. wire had more than enough impedance to allow the hood to be transparent to the ignition pulses. By putting short braided cables on both hinges and ensuring a good ground through the latch mechanism, the car finally passed the Canadian EMI tests.

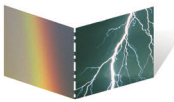
A return path is not an ocean of zero impedance. Some engineers think it would be more illustrative to draw every ground as a wire because even copper planes have impedance. This approach might make audio engineers more circumspect about using single-point grounding. The problem is that every audio circuit must work at 1.2

GHz—not to pass any signal but to reject noise from cell-phone radiation. By discarding ground planes in favor of thin traces that wind back to a single-point ground, some audio engineers get slightly better distortion measurements, but at the expense of poor immunity to RF (Reference B). Remember that every one of those long, spindly "ground" wires is an antenna.

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You use one optocoupler as a reference; the second transmits the dc level across the isolation boundary. Avago's HCNR200 optocoupler has one LED and two photodiodes that you can use for a referenced servo system; Solid State Optronics offers a similar device (Figure 3 and Reference 6). Like all other isolators, optocouplers also have a phase delay, and you may have to compensate for it (Reference 7).

Texas Instruments' ISO124 and Analog Devices' AD204 op amps, both with built-in isolation, also provide approaches for bringing analog signals across isolation. The ISO124 uses capacitors formed by metal plates on the lead frame, and the package's molding compound acts as a dielectric. The AD204 uses transformers rather than capacitors to provide the same results. The Analog Devices product also has a power section that sends power across the boundary for the other side of the device and for any other ancillary functions.

If you can possibly build your system to pass digital representations of your analog signals across the isolation boundary, then you can take advantage of a slew of newer digital-isolator parts, which represent a new trend in system design and data acquisition. "I still get people who want to talk about analog isolation," says Tim Lafferty, a product-marketing manager at Texas Instruments. "I show them the ISO124, but I explain that [digital isolation] is really the way that the world is going."

The idea is to put a serial ADC on the isolated side of your design and feed it isolated power that can also supply the op amps or signal-conditioning circuitry. You then use digital isolators to bring the ADC data back across your isolation boundary. "You might use these isolated amplifiers in a feedback system, such as a motor drive," says Analog Devices' Krakauer. "But, more and more, those feedback systems are going digital."

"The ADC has worked its way closer and closer to the sensor bridge in almost every application," says NVE's

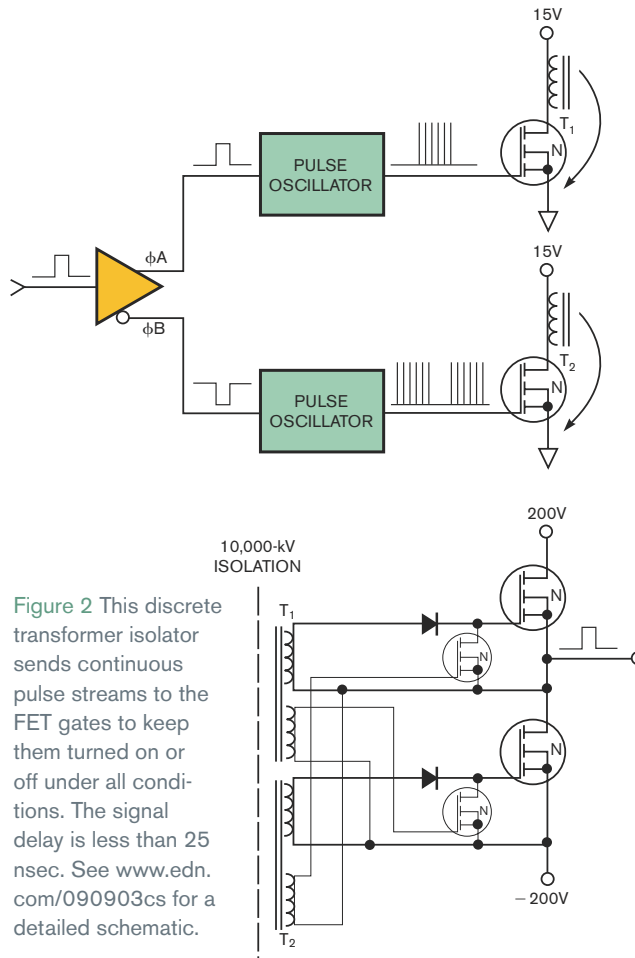


Figure 2 This discrete transformer isolator sends continuous pulse streams to the FET gates to keep them turned on or off under all conditions. The signal delay is less than 25 nsec. See [www.edn.com/090903cs](http://www.edn.com/090903cs) for a detailed schematic.

Templeton, who notes that you can use analog isolation in voltage-controlled systems, such as those for thermal and pressure control, but delta-sigma modulators are replacing isolation op amps in even those applications. Keep in mind, though, that you must build an isolated power supply for the front end of a digital system, whereas the AD204/210 parts have built-in isolated power.

The oldest digital isolators, optocouplers, work at 50 Mbps; include analog optocouplers that drive integrated digital gates; and are available from dozens of companies, including Vishay and Toshiba. Several companies, including Fairchild and International Rectifier, make isolators for power-supply feedback. Clare and Crydom offer another class of isolation products, solid-state relays, for ac-line control. Several companies also offer digital isolators using capacitive, inductive, and other isolation methods. Vendors of these systems claim that they consume less power and fit into smaller packages than do optical isolators.

You should pay attention to the method by which digital isolators encode

the input signal and carry it across the boundary. TI integrates two differential channels in its capacitive isolators because it is impossible to send a dc level across a capacitor (Figure 4). The company's new isolator line includes well-matched die capacitors to provide common-mode rejection of 50-kV transient spikes. The ac channel takes the edges of the data stream across the capacitive boundary with no encoding, making the chips speedy. The second channel encodes the dc level of the input signal and sends it across two more capacitors as a differential signal. Decoding of this signal takes place in the receiver chip and provides the dc information if the signal lingers at 0 or 1V.

Also consider whether an asynchronous clock performs the encoding that brings the signal across the boundary. Several vendors warn that these "level-triggered" systems

can change the shape and duration of fast pulses. In "edge-triggered" systems, the logic is not simply gating a free-running clock. Instead, the gates act as oscillators that emit a pulse within a gate delay of the incoming data and then continue to pulse until the input signal goes away. Simply gating a fast-enough pulse train across the boundary can be an effective approach. For example, Silicon Labs uses an internal asynchronous, 700-MHz RF signal to encode input data, and the pulse-width errors are in the nanosecond range (Figure 5).

Linear Technology has leveraged its module-building expertise to incorporate power and signal isolation in a module that transmits RS-485-bus signals across a 2500V boundary (Figure 6). This approach may appeal to many engineers because it is a repackaging of time-tested technology. The module does not represent the company's only foray into isolation, however; years ago, it introduced the LTC1535 RS-485 isolator. The device uses capacitors on the lead frame to bring the signal across the isolation boundary. The new LTM2881

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$\mu$ Module uses transformers built into a PCB (printed-circuit board).

Some digital parts comply with high-level protocols, such as I<sup>2</sup>C (inter-integrated circuit), RS-485, CAN (controller-area network), and USB (Universal Serial Bus), and several vendors make parts that comply with these standards. For example, Analog Devices' ADuM4160 iCoupler provides an isolated USB system, and other products provide isolated I<sup>2</sup>C interfaces. Texas Instruments recently introduced the ISO1050 for CANbus applications in cars or factories. A hybrid digital/analog isolation technique uses an isolated delta-sigma modulator followed by a lowpass filter. In this case, you convert an analog signal into a PWM digital pulse train, send it across the boundary, and then use a filter to turn the PWM signal back into the analog domain. Be aware that you must create an isolated power supply to feed the front end of the modulator. For example, Avago's ACPL-785J optically isolated delta-sigma modulator (Figure 7) lacks a lowpass filter, but you can use a digital filter to get a representation of the analog signal, or you can put your own lowpass filter on the output.

Similarly, Texas Instruments' AMC-

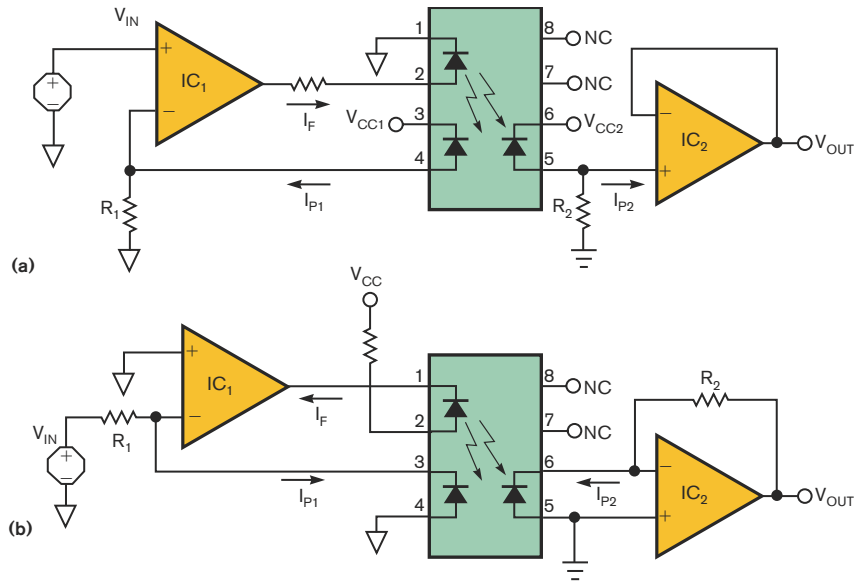


Figure 3 You can compensate for aging in optocouplers by using a dual-phototransistor part in a servo loop with photoconductive (a) or photovoltaic (b) operation (courtesy Solid State Optonics).

1203 delta-sigma modulator has no built-in filter. The 16-bit, 10-MHz AMC1203 also feeds the AMC1210 digital filter to allow you to create an isolated resolver-interface circuit. The device provides 4000V isolation and comes with agency approvals. Analog Devices' 16-bit-resolution, 20-MHz AD7401 sigma-delta

modulator also can bring an analog signal across an isolation boundary and, in compliance with UL1577, can stand off 3750V for one minute.

### ISOLATION METHODS

Vendors use a number of techniques, including RF, optical, capacitive, trans-

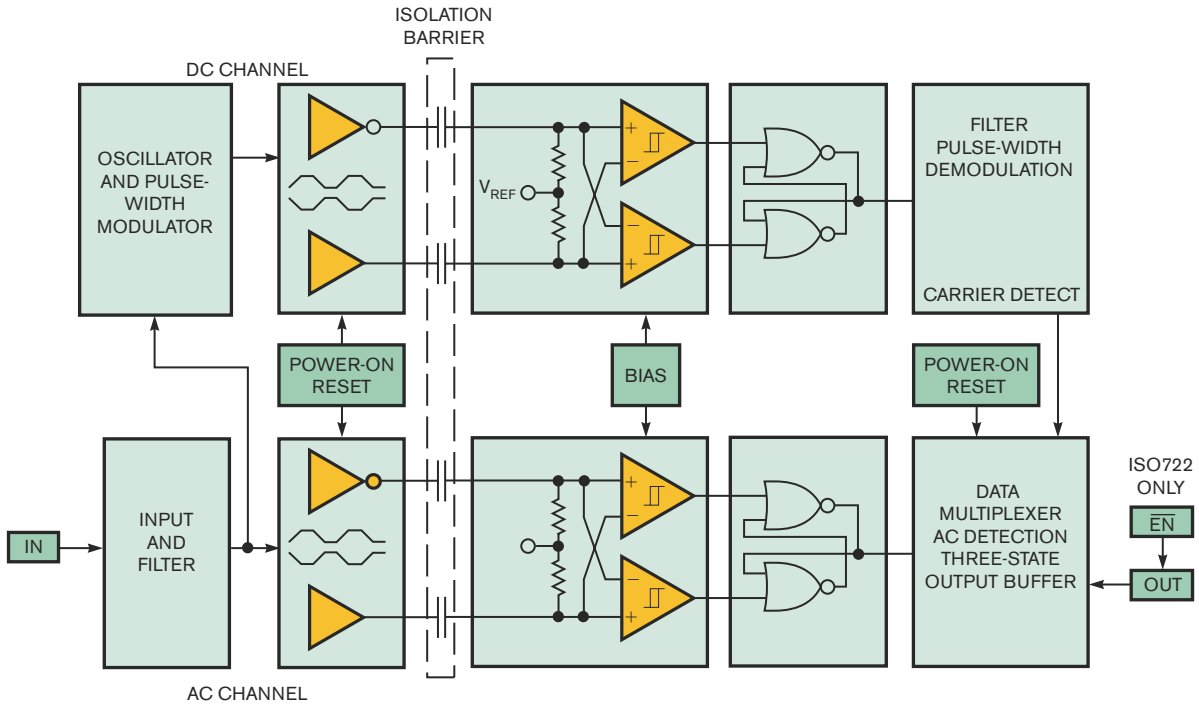


Figure 4 Texas Instruments uses an ac differential channel and a dc differential channel in its new digital isolators. The isolation barrier is on-die glass, and the coupling is capacitive.



## HIGH JITTER

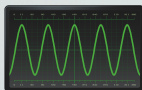
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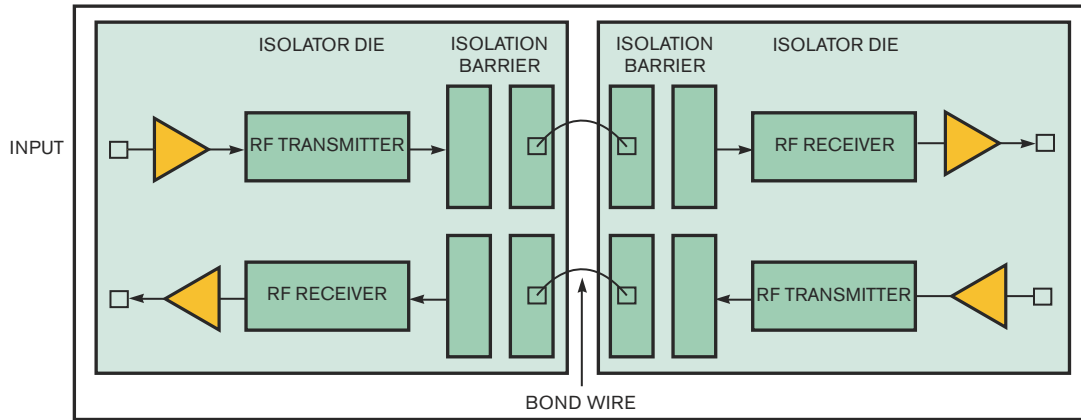


Figure 5 This Silicon Labs isolator uses RF across an on-die-glass isolation barrier. The modulation frequency is 700 MHz.

former, and GMR (giant-magneto-resistive) sensing, to provide isolation in their products. The insulators the companies use are as varied as the number of dielectric compounds. According to Texas Instruments' Lafferty, the properties of the insulation in a part may translate to its performance and long-term reliability. "One of TI's objectives [for] digital isolators was to make isolation completely out of semiconductor materials in a semiconductor-[manufacturing] flow," he says. Lafferty claims that this approach makes the company's new digital-isolator line more repeatable, more dependable, and more reliable.

Analog Devices' iCoupler line instead uses transformer coupling with polyamide film as the dielectric (Figure

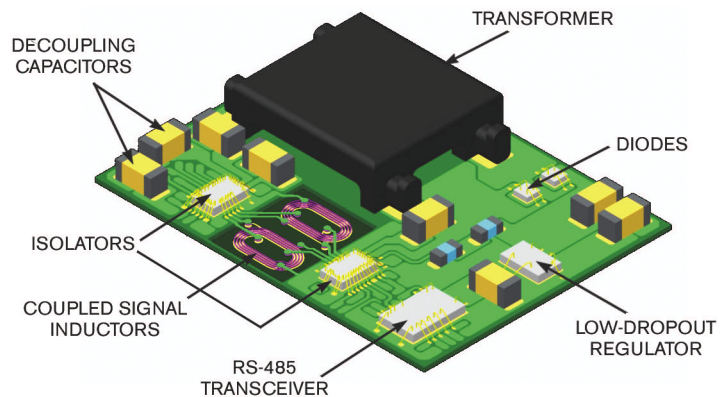


Figure 6 Linear Technology's LTM2881 complete isolated RS-485 subsystem also provides isolated power. The isolation barrier is FR (flame-retardant)-4 PCB material, and the coupling is inductive. It resides in an 11.25×15×2.8-mm package.

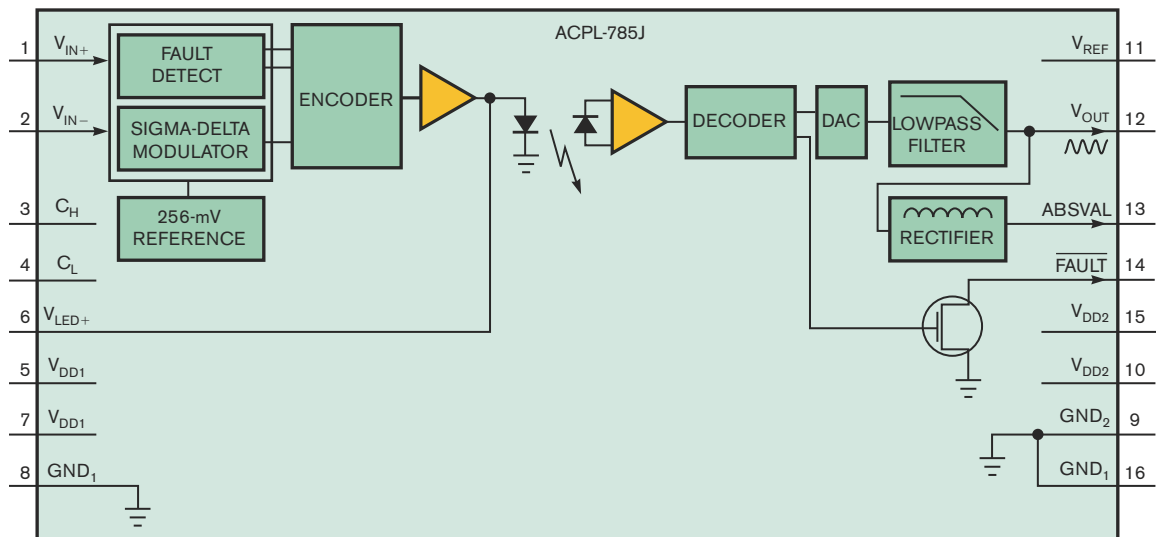


Figure 7 Avago's isolated delta-sigma modulator has a built-in lowpass filter so that you can bring analog signals across an isolation boundary. The coupling is optical, and the dielectric is a clear mold compound.



8), whereas Texas Instruments uses capacitive coupling with glass as the insulator in the ISO72xx. Linear Technology uses discrete capacitors on the lead frame of its LT1535, and its new LT2881 uses PCB material as the isolation for spiral transformers. In contrast, NVE uses electron spin across a proprietary polymer film to convey the signal (Figure 9). NVE's approach uses spin valves employing GMR. A huge change in resistance occurs when you expose the devices to a magnetic field. The company builds parts with a small coil to generate a magnetic field and GMR sensors on the other side of the boundary. Analog Devices has also introduced a transformer-coupled line that uses die glass as the insulator. "If safety isn't important [and] if the only thing customers care about is breaking a ground loop or reducing noise, then they don't need the high-isolation capability of our standard products," says Krakauer. The parts use the same spiral-transformer technology as the high-voltage parts. With these new parts, 5 microns of silicon dioxide separate the transformer windings in-

stead of 20 microns of polyamide in the earlier parts. Designers can also use the company's transformer technology to send power across the boundary, resulting in higher system integration.

Silicon Labs creates an RF signal inside the chip and beams it over to a receiver antenna. The dielectric is glass that grows on the die. The company also uses on/off keying for modulation. "The benefit of this [approach] is that the output always unconditionally follows the input," says Javed, noting that this approach makes the system more immune to noise interference than parts that use latch-based or pulse topologies. Acoustic coupling is yet another approach to isolation (Reference 7).

### SELECTING A TECHNOLOGY

The overriding consideration in selecting any isolator is the standoff voltage. The need for UL or international-standard certification may—more than any other factor—determine the part selection. You can get UL approval for designs that use non-UL-listed parts, but it is a much more time-consuming pro-

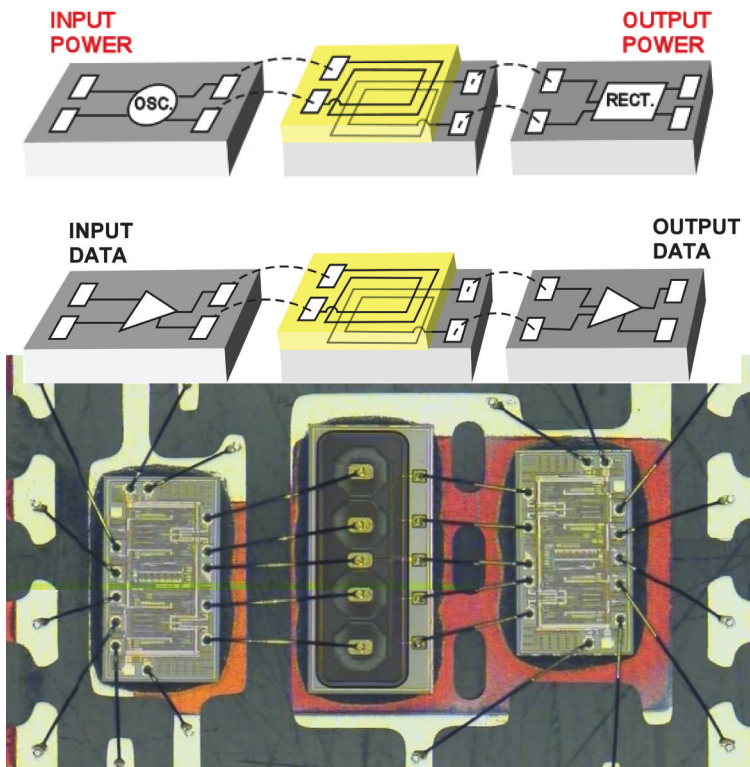


Figure 8 Analog Devices' iCoupler technology uses tiny transformers isolated with polyamide film. The transformers can also send power across the boundary.

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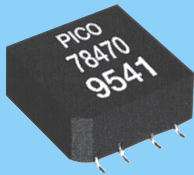
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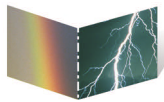
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cess. You must prove to UL that the isolation boundary is adequate. It is far easier to select isolator parts that have the safety approvals.

The first decision to make with isolators is to consider whether you must bring an analog signal back across the isolation boundary. If the signals are slow enough and you have the budget, using the legacy ISO124 or AD204 is an acceptable approach. You should always consider using optocouplers because they are ubiquitous, but you must either live with their inherent aging problems or provide a reference servo design that compensates for those problems. Delta-sigma modulators from Avago, Analog Devices, and Texas Instruments are available for designs requiring higher bandwidths.

These units bring digital signals across a boundary, but you can then make it analog using a simple lowpass filter. TI uses capacitive coupling, Analog Devices uses transformers, and Avago uses optocouplers. Because the signal across the barrier is digital in Avago's products, optocoupler aging is not a problem.

Most digital-isolation applications operate at speeds of 1 to 50 Mbps. If speed is not your first concern, then power may be. Optocouplers in a logic-low state are not also driving the LED, in which case the drive current is 0A. You may be able to design your system to take advantage of that feature. NVE offers a device that provides the magnet-coil inputs with no interposed driver chip. "With these coil inputs, the signal provides the power itself," says Templeton. "You don't need to supply any power on the input side." In this way, you can drive the coil in any way that you choose—perhaps in a way that saves a significant amount of power. Most of the alternative methods to optocoupling claim lower power consumption. If your application operates at 1 to 50 Mbps, you have many technologies from which to choose. One important spec may be transient immunity. "If there is one parametric Achilles' heel that you must watch out for, it is the

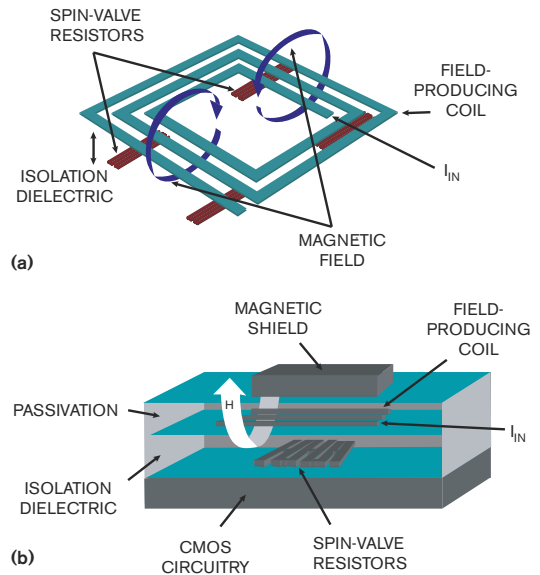


Figure 9 NVE parts use GMRs and a driving coil. Coupling is magnetic, and the dielectric is a polymer film (a). Parts are available with and without an integrated driver circuit for the coil (b).

$dV/dt$  [change in voltage over time] of the common-mode voltage," warns TI's Jerry Steele, a strategic-development engineer at Texas Instruments. This test slews one side of an isolator across a large voltage difference while you determine whether the data is still valid. Vendors routinely specify parts at 25 kV/ $\mu$ sec. Texas Instruments points out that its isolators work properly with a 50-kV/ $\mu$ sec transient across the boundary.

Another consideration is electromagnetic susceptibility. Texas Instruments claims that its capacitive isolation has greater immunity to magnetic fields than do other technologies. Analog Devices, however, says that the level of magnetic fields that would cause an error in its part would have to be so huge that it would ruin the signal integrity of every other part and trace in your design. NVE bases its isolators on a magnetic field but says that they are close-coupled and shielded and that strong magnetic fields impinge on the isolator in only a few applications. "[Magnetic fields] just don't come up [with our customers]," says Dan Baker, president and chief executive officer of NVE. "Our device has more practical aspects of an EMC [electromagnetic-compatibility] footprint, immunity to external

fields, and [reduced] transmitted external fields.”

Whereas you might think an isolator from Silicon Labs would be too sensitive to external fields because it is an RF system, you might want to reconsider. “We tried several technologies and found the Silicon Labs parts to be best for immunity and radiation in our application,” says John James, a lead engineer at Crossbow Technology. You must characterize how the data flowing across your isolator affects the ability of your product to pass FCC (Federal Communication Commission) and CE (Conformité Européenne) radiated-EMI tests.

### TRADE-OFFS

As with a lot of other complex decisions, when choosing an isolator, you must divide what you need from what you want. The requirement for a certain voltage standoff or UL listing narrows your search. If a compact footprint is a requirement, shy away from optoisolator circuits and instead look at integrated products from Texas Instruments, Silicon Labs, and others. For designs requiring a USB interface, Analog Devices offers a system that can use two chips to give you isolated data and isolated USB 5V power. When cost is a concern, consider legacy optoisolators from Avago, Vishay, and NEC. The fact that these devices are legacy products means that you won't have to worry about their obsolescence. All the companies making digital isolators pledge to keep them in their portfolios for as long as a decade, but using optocouplers in standard package pinouts is a safe bet for ensuring that obsolescence does not ruin your design.

When you have listed necessities and desires, you will reach a decision on a product that is specific to your design. A part's EMI/RFI (radio-frequency-interference) immunity, magnetic fields, pulse-width fidelity, and long-term reliability all play into your decision. Set up test scenarios specific to your application and test the part in an environment that proves that the part will work for you.

Remember that it is sometimes better to keep things in the analog domain and use legacy parts. No matter whether you use analog or digital isolators, you should understand how the parts work. Capacitor,

transformer, RF, optical, acoustic, and GMR techniques are all available, and they all behave differently. One exciting development is the expansion of an isolator's operating-temperature range into the military realm. All of these advances build on a solid foundation of isolation techniques that manufacturers have perfected over the decades. **EDN**

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# Characterizing noise in high-performance voltage-reference ICs

MEASURING THE NOISE PERFORMANCE OF A MODERN VOLTAGE REFERENCE REQUIRES SPECIAL MEASUREMENT TECHNIQUES.

Voltage-reference stability and noise frequently define the measurement limits of instrumentation systems. In particular, reference noise often sets stable resolution limits. Reference voltages have decreased with the continuing drop in system power-supply voltages, making reference noise increasingly important. The compressed signal-processing voltage range mandates a commensurate reduction in reference noise to maintain resolution. Noise ultimately translates into quantization uncertainty in ADCs, introducing jitter in applications such as scales, inertial navigation systems, infrared thermography, digital voltmeters, and medical-imaging apparatus. A new voltage reference has the accuracy and temperature coefficient typical of high-grade, low-voltage references. However, no other low-voltage electronic reference can equal the new device's 0.1- to 10-Hz noise (Table 1, pg 40).

You must use special techniques to verify the part's extremely low noise. A straightforward approach appears simple, but the practical implementation represents a measurement with a high

order of difficulty (Figure 1). This 0.1- to 10-Hz noise-testing scheme includes a low-noise preamplifier, filters, and a peak-to-peak noise detector. The preamplifier's 160-nV noise floor requires special design and layout techniques. A forward gain of 1 million permits conventional instruments to provide a readout.

The 1300- $\mu$ F-capacitor/1.2-k $\Omega$ -resistor combination strips the reference's dc potential (Figure 2). The ac content goes to transistor  $Q_1$ . Amplifier  $A_1$  dc-stabilizes low-noise JFETs  $Q_1$  and  $Q_2$ . Amplifier  $A_2$  provides a single-ended output. Resistive feedback from  $A_2$  stabilizes the configuration at a gain of 10,000.  $A_2$ 's output routes to amplifier-filter  $A_3/A_4$ , which provides a 0.1- to 10-Hz response at a gain of 100. Amplifiers  $A_5$  through  $A_8$  comprise a peak-to-peak noise detector readout for a DVM (digital voltmeter) at a scale factor of 1V/ $\mu$ V. The peak-to-peak noise detector provides a highly accurate measurement, thus eliminating a tedious interpretation of an oscilloscope display. The indicated output instantaneously supplies a noise value to a monitoring oscilloscope. The 74C221 one-shot, which the oscilloscope's sweep gate triggers, resets the peak-to-peak noise detector at the end of each 10-sec oscilloscope sweep. For a list of some useful low-level amplifiers for setting up and troubleshooting the circuit in Figure 2, see sidebar "High-sensitivity, low-noise amplifiers").

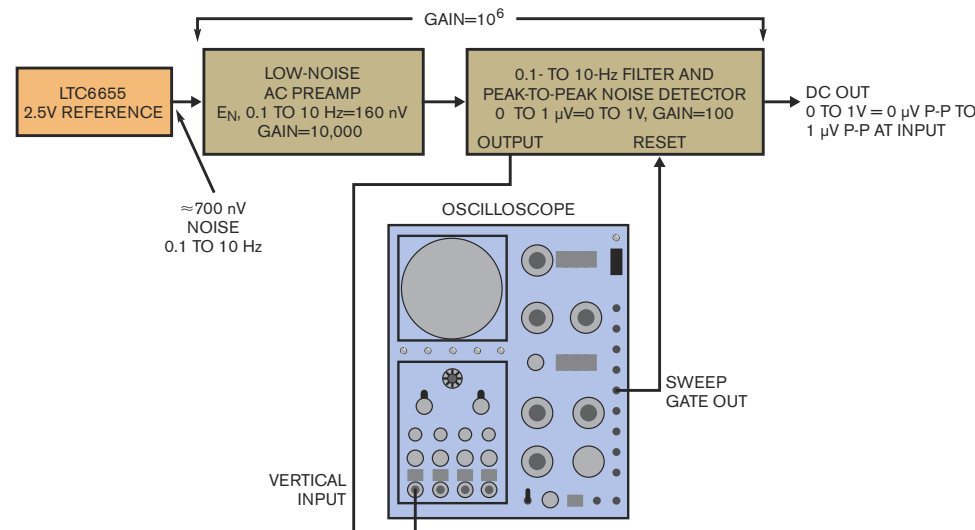
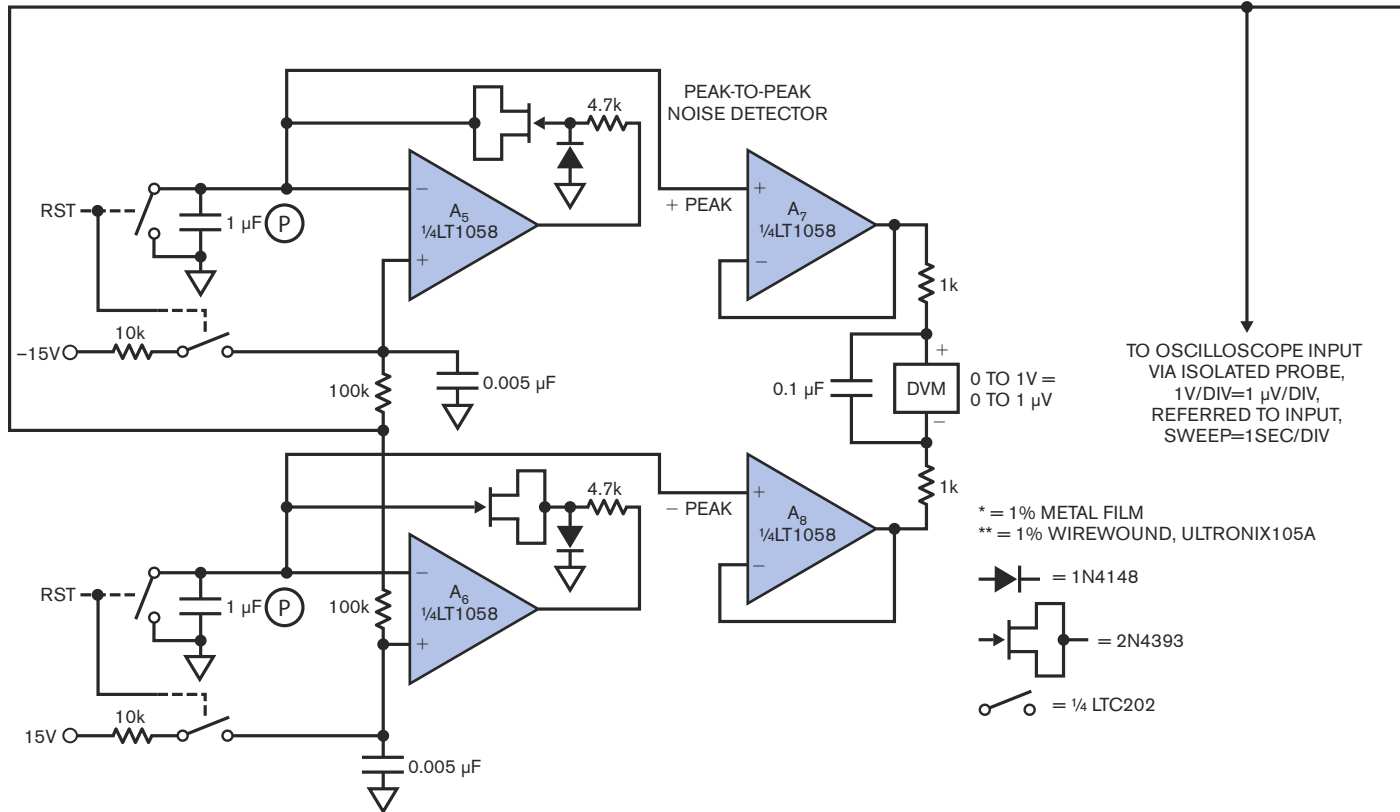
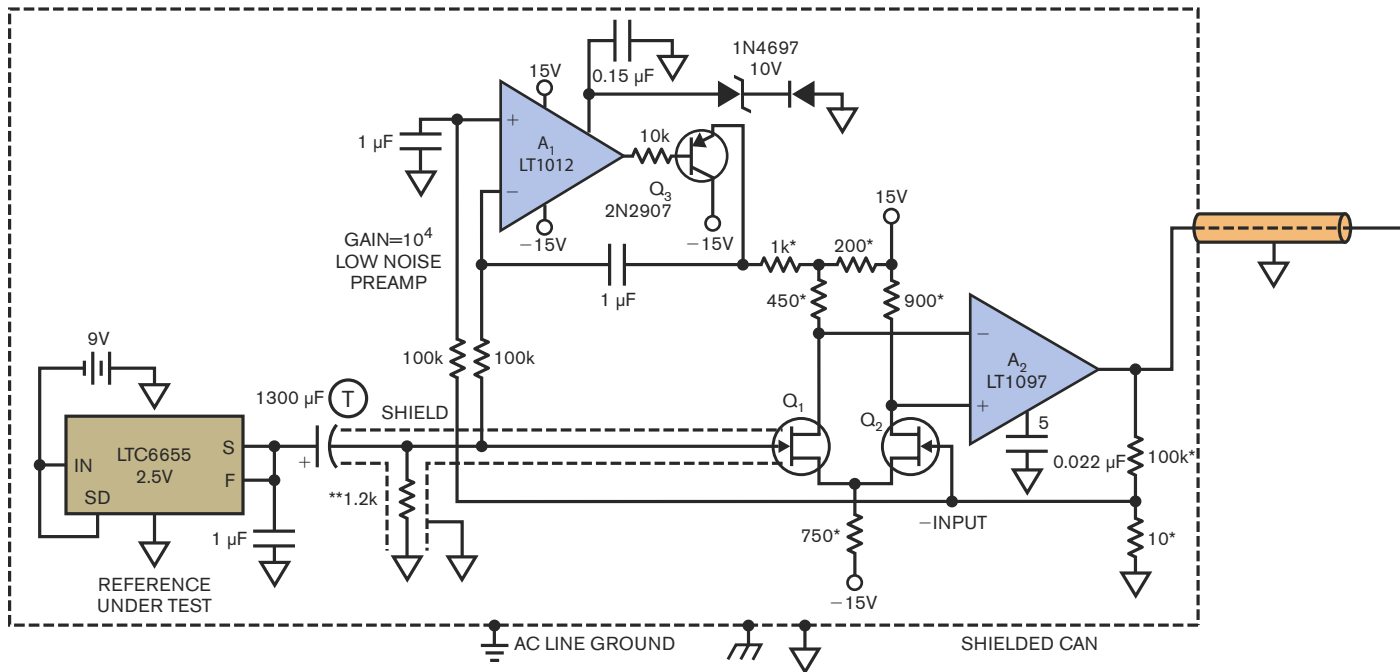


Figure 1 A conceptual 0.1- to 10-Hz noise-testing scheme includes a low-noise preamplifier, a filter, and a peak-to-peak noise detector.

order of difficulty (Figure 1). This 0.1- to 10-Hz noise-testing scheme includes a low-noise preamplifier, filters, and a peak-to-peak noise detector. The preamplifier's 160-nV noise floor requires special design and layout techniques. A forward gain of 1 million permits conventional instruments to provide a readout.

You must select the highly specialized 1300- $\mu$ F input capacitor for leakage. Otherwise, resultant errors can saturate the input preamplifier or introduce noise. You must use the highest-grade wet-slug 200°C-rated tantalum capacitors. The capacitor operates at a small fraction of its rated voltage at room temperature, resulting in lower leakage than its specification indicates. When evaluating leakage, you should note that



**Figure 2** In the circuit implementation of the conceptual noise-testing scheme,  $A_1$  through  $Q_3$  dc-stabilize the thermally lagged  $Q_1/Q_2$  low-noise JFET pair.  $A_3$  and  $A_4$  form a 0.1- to 10-Hz bandpass filter. Total gain referred to the preamplifier's input is  $10^6$ .

the capacitor's dielectric absorption requires a 24-hour charge time to ensure meaningful measurements (**Figure 3**). You determine capacitor leakage by using the following procedure:

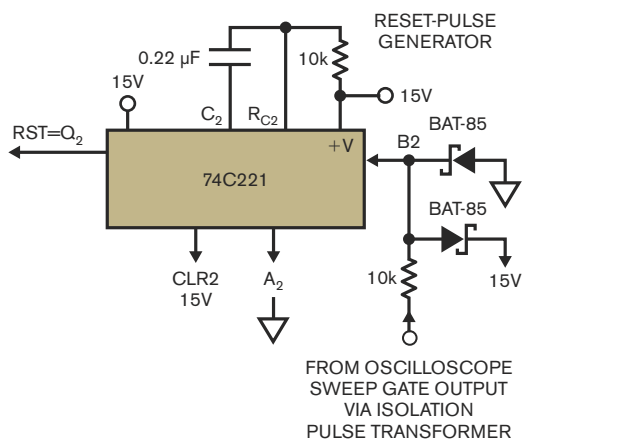
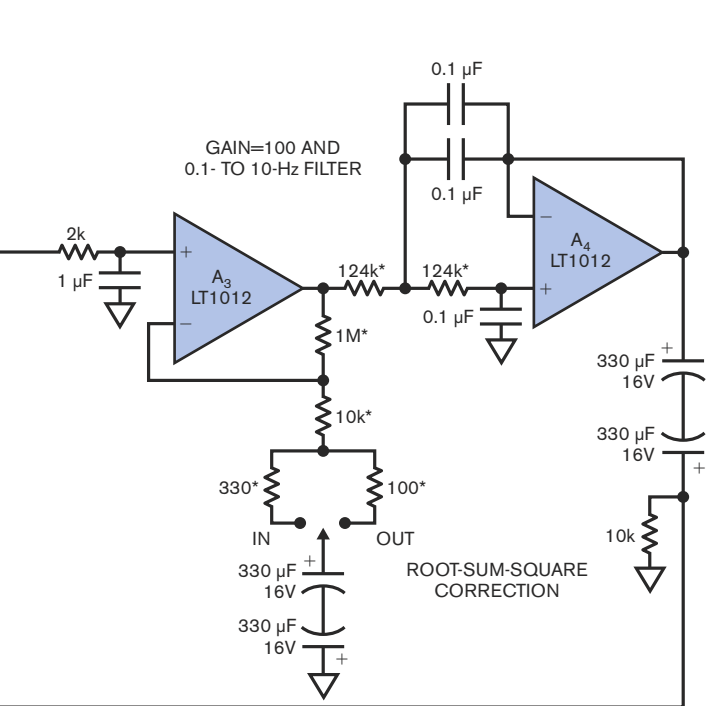
1. Turn off the microvolt meter.
2. Connect the 3V battery stack.

3. Wait 24 hours.

4. Turn on the microvolt meter.

5. Read the capacitor's leakage, where 1 nA equals 1  $\mu$ V.

The yield to the required 5-nA leakage should exceed 90%. This high yield is most welcome because the specified capaci-



$Q_1, Q_2$  = THERMALLY MATED  
2SK369 (MATCH  $V_{GS}$  10%) OR  
LSK389 DUAL THERMALLY LAG

(T) = TANTALUM, WET SLUG  
 $I_{LEAK} < 5$  nA

(P) = POLYPROPYLENE

$A_4$  330- $\mu$ F OUTPUT CAPACITORS =  
<200-nA LEAKAGE AT 1V<sub>DC</sub> AT 25°C

tors sell for almost \$400 each. A more palatable alternative may exist, however. Selected commercial-grade aluminum electrolytics can approach the required dc leakage, although their aperiodic noise bursts are concerning. The input capacitor and its associated low-noise, 1.2-k $\Omega$  resistor are fully shielded against external-noise pickup.

You must carefully prepare the low-noise, gain-of-10,000 preamplifier because it is crucial to the noise measurement.

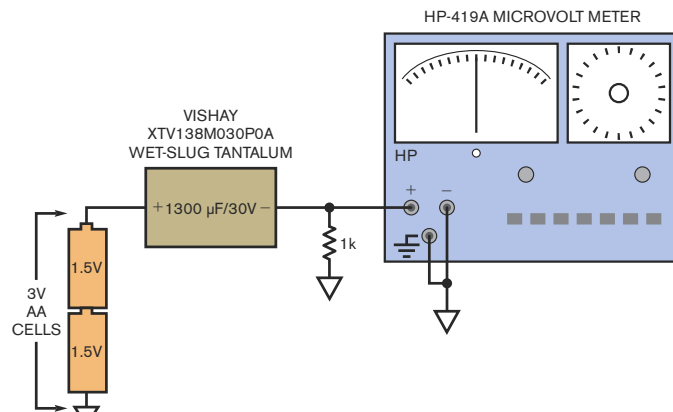


Figure 3 Use this test setup to select input capacitors with less than 5 nA of leakage current.

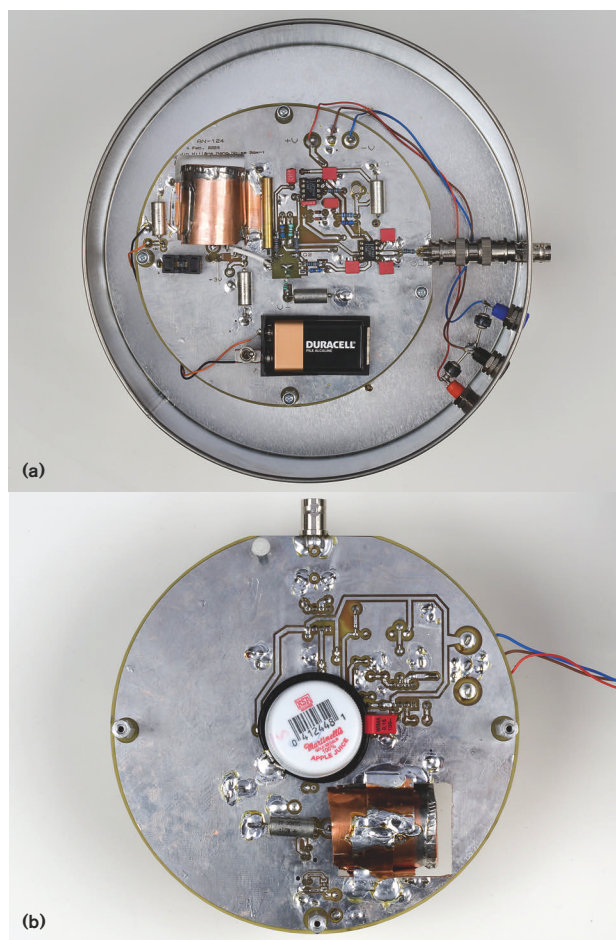
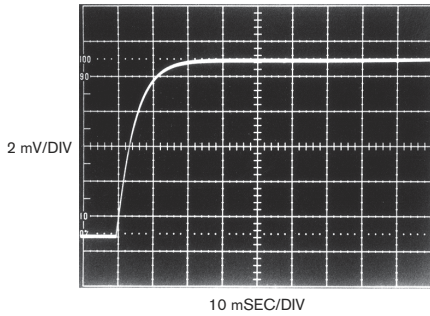
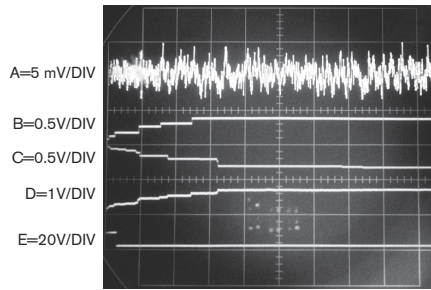


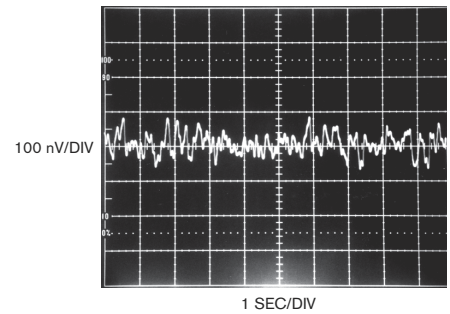
Figure 4 The preamplifier board's top side (a) includes a shielded input capacitor (upper left) and input resistor (upper center left). The stabilized JFET input amplifier occupies the upper center right. The output stage adjoins the BNC fitting. The reference under test resides in a socket below the input capacitor. The circuit's  $\pm 15$ V power enters the shielded enclosure through banana jacks (extreme right). A 9V battery (bottom) supplies the reference under test. The board's bottom side (b) includes an epoxy-filled plastic cup that contains the JFETs and provides thermal mating and thermal time lag.



**Figure 5** The preamplifier's rise time of 10 msec indicates a 35-Hz bandwidth, ensuring that the circuit feeds the entire 0.1- to 10-Hz noise spectrum to the succeeding filter stage.



**Figure 6** The peak-to-peak noise detector's waveforms include  $A_3$ 's input-noise signal (Trace A), the peak-detector output of  $A_7$ 's positive signal (Trace B), the peak-detector output of  $A_8$ 's negative signal (Trace C), and the DVM's differential input (Trace D). The oscilloscope supplies the reset pulse (Trace E).



**Figure 7** Low-noise circuit-layout techniques ensure accurate measurement. A 3V battery replaces the reference under test, yielding the 160-nV, 0.1- to 10-Hz noise floor. The circuit corrects for this noise floor at amplifier  $A_3$ .

## High-sensitivity, low-noise amplifiers

**TABLE A** HIGH-SENSITIVITY, LOW-NOISE AMPS

Instrument type	Manufacturer	Model	-3-dB bandwidth	Maximum sensitivity/gain	Availability	Comments
Differential amplifier	Tektronix	1A7/ 1A7A	1 MHz	10 $\mu$ V/div	Secondary market	Requires 500 series mainframe, settable bandstops
Differential amplifier	Tektronix	7A22	1 MHz	10 $\mu$ V/div	Secondary market	Requires 7000 series mainframe, settable bandstops
Differential amplifier	Tektronix	5A22	1 MHz	10 $\mu$ V/div	Secondary market	Requires 5000 series mainframe, settable bandstops
Differential amplifier	Tektronix	ADA-400A	1 MHz	10 $\mu$ V/div	Current production	Stand-alone with optional power supply, settable bandstops
Differential amplifier	Preamble	1822	10 MHz	Gain: 1000	Current production	Stand-alone, settable bandstops
Differential amplifier	Stanford Research Systems	SR-560	1 MHz	Gain: 50,000	Current production	Stand-alone, settable bandstops, battery or line operation
Differential amplifier	Tektronix	AM-502	1 MHz	Gain: 100,000	Secondary market	Requires TM-500 series power supply, settable bandstops

Table A lists some useful low-level amplifiers for setting up and troubleshooting. The table lists both oscilloscope plug-in amplifiers and stand-alone types. Two major restrictions apply. The filters in these units are single-pole types, resulting in somewhat pessimistic bandwidth cutoffs. Additionally, the amplifiers do not include 10-Hz,

lowpass-frequency filters, although you can easily modify them to provide this capability. Table B lists four amplifiers with the necessary modification information (references A, B, C, and D).

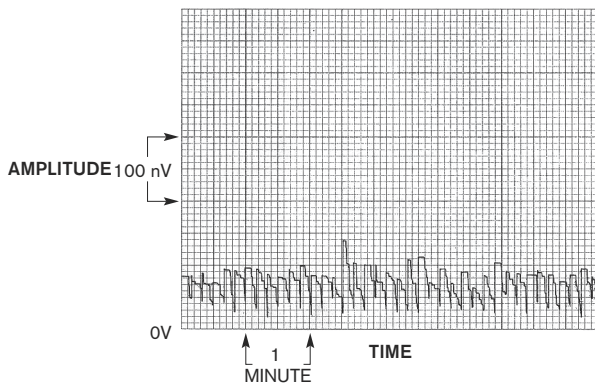
**TABLE B** MODIFICATION INFORMATION

Manufacturer	Model	Modification
Tektronix	1A7	Parallel C370A with 1 $\mu$ F
Tektronix	1A7A	Parallel C445A with 1 $\mu$ F
Tektronix	7A22	Parallel C426H with 3 $\mu$ F
Tektronix	AM502	Parallel C449 with 3 $\mu$ F

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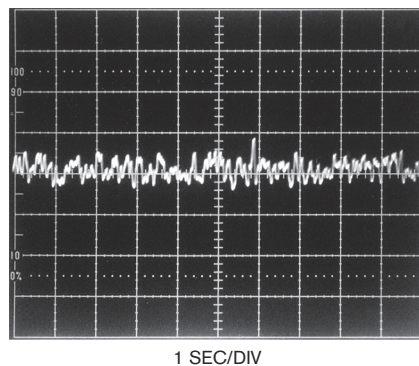
- A** *Type 1A7 Plug-In Unit Operating and Service Manual*, Tektronix Inc, 1965.
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- C** *Type 7A22 Differential Amplifier Operating and Service Manual*, Tektronix Inc, 1969.
- D** *AM502 Differential Amplifier Operating and Service Manual*, Tektronix Inc, 1973.





**Figure 8** Long-term noise-floor measurement at the peak-to-peak noise detector's output shows less than 160 nV of noise, with a reset every 10 sec. A 3V battery replaces the reference under test for this test.

JFETs  $Q_1$  and  $Q_2$  differentially feed  $A_2$ , forming a simple low-noise op amp. The  $100\text{-k}\Omega/10\Omega$  pair provides feedback that sets the closed-loop gain at 10,000. Although  $Q_1$  and  $Q_2$  have low-noise characteristics, they suffer from high offset and drift.  $A_1$  corrects these deficiencies by adjusting  $Q_1$ 's channel current through  $Q_3$  to minimize the  $Q_1/Q_2$  input difference.  $Q_1$ 's skewed drain values ensure that  $A_1$  can capture the offset.  $A_1$  and  $Q_3$  supply the necessary current into  $Q_1$ 's channel to force offset within about  $30\ \mu\text{V}$ . The JFET's gate-to-source voltage



**Figure 9** The LTC6655's 0.1- to 10-Hz noise measures 775 nV in a 10-sec sample time.

can vary over a 4-to-1 range. Because of this situation, you must hand-select the JFETs for 10% gate-to-source voltage matching. This matching allows  $A_1$  to capture the offset without introducing significant noise. You must enclose  $Q_1$  and  $Q_2$  in an epoxy pot to thermally mate them and ensure a time-lag response to a time constant much greater than  $A_1$ 's dc stabilizing-loop rolloff. This thermal management of the JFETs prevents offset instability and hunting in  $A_1$ 's stabilizing loop from masquerading as low-frequency noise.

A shielded can completely encloses the  $A_1/Q_1/Q_2/A_2$  assembly and the reference under test (**Figure 4**). You should pro-

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vide additional shielding to the input capacitor and resistor. The resistor's wirewound construction has low noise but is susceptible to stray fields. The reference under test is socketed below the large input-capacitor shield and the JFET input amplifier's associated components. Because  $Q_3$  is a heat source, you should place it away from the JFET PCB's (printed-circuit board's) lands, which prevents convection currents from introducing noise. The amplifier's  $\pm 15V$  power enters the enclosure through banana jacks. A 9V battery powers the reference under test to minimize noise and ensure freedom from ground loops.

The gain-of-100 filter and the peak-to-peak detector circuitry occupy a separate board outside the shielded can. You should minimize board leakage to the peak-detecting capacitors with guard rings or a flying-lead/Teflon standoff construction. Peak-to-peak-detector design considerations include using JFETs

as peak-trapping diodes to obtain lower leakage than conventional diodes afford. Diodes at the FET gates clamp reverse voltage, further minimizing leakage. Diode-connected JFETs' superior leakage derives from their small gate-channel junction. In general, JFETs leak a few picoamperes, whereas common signal diodes, such as the 1N4148, leak approximately 1000 times more current, which you measure in nanoamperes at 25°C.

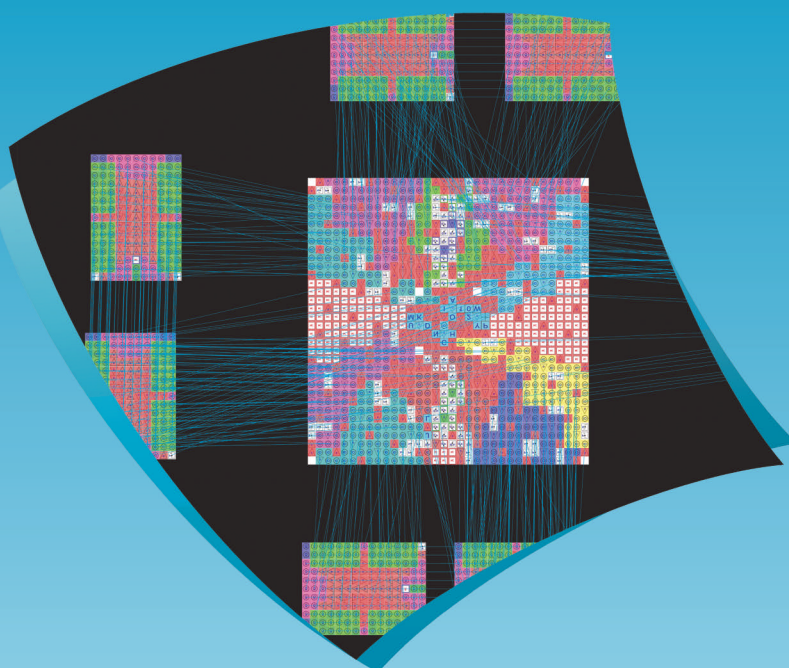
The peak-storage capacitors have a highly asymmetric charge-discharge profile, necessitating the use of low-dielectric-absorption polypropylene capacitors. Teflon and polystyrene dielectrics are even better, but Teflon capacitors are expensive and have excessively large size at 1  $\mu F$ , and the sole manufacturer of polystyrene film has ceased production. Oscilloscope connections through galvanically isolated links prevent ground-loop corruption. An isolated probe supplies the oscilloscope's input signal. You should interface to the sweep-gate output with an isolation-pulse transformer (see sidebar "Power, grounding, and shielding considerations" in the Web version of this article at [www.edn.com/090903ms4338](http://www.edn.com/090903ms4338)).

You must characterize circuit performance before measuring the reference under test's noise. You can verify the pre-amplifier stage for greater-than-10-Hz

**TABLE 1 LTC6655 SPECIFICATIONS**

Specification	Limits
Output voltages (V)	1.25, 2.048, 2.5, 3, 3.3, 4.096, 5
Initial accuracy (%)	0.025, 0.05
Temperature coefficient (ppm/°C)	2, 5
0.1- to 10-Hz noise	0.775 $\mu V$ at an output voltage of 2.5V, peak-to-peak noise is within this figure in 90% of 1000 10-sec measurement intervals
Additional characteristics	5-ppm/V line regulation, 500-mV dropout, shutdown pin, supply current is 5 mA, input voltage is the output voltage plus 0.5V to a maximum of 13.2V, sink and source output current is $\pm 5$ mA, short-circuit current is 15 mA

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bandwidth by applying a 1- $\mu$ V step at its input with the reference disconnected while monitoring  $A_2$ 's output. A 10-msec rise time indicates a 35-Hz response (Figure 5). This approach ensures that the circuit supplies the entire 0.1- to 10-Hz noise spectrum to the succeeding filter stage. Oscilloscope plots reveal the peak-to-peak-noise-detector operation (Figure 6).

You measure the noise floor of the circuit by replacing the reference under test with a 3V battery stack. Dielectric-absorption effects in the large input capacitor require a 24-hour settling period before you take a measurement. The circuit's oscilloscope output shows 160-nV, 0.1- to 10-Hz noise in a 10-sec sample window (Figure 7). Because noise adds in root-sum-square fashion, this output represents an approximately 2% error in the LTC6655's expected 775-nV noise figure. Placing the root-sum-square-correction switch of Figure 2 in the appropriate position during reference testing accounts for this term. The resultant 2% gain attenuation corrects the reference under test's output-noise reading to the first order. A strip-chart recording of the peak-to-peak noise detector's output over six minutes shows less than 160-nV test-circuit noise (Figure 8). The circuit resets every 10 sec. A 3V battery biases the input capacitor, replacing the LTC6655 for this test.

You can observe the LTC6655 noise after the 24-hour dielectric-absorption soak time (Figure 9). With the root-sum-square correction enabled, the noise is within 775 nV p-p in this 10-sec sample window. The circuit's verified low-noise floor makes it highly likely that this data is valid. You can apply this approach to measuring any 0.1- to 10-Hz noise source, although you should re-establish the root-sum-square error-correction coefficient for any given noise level. **EDN**

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## AUTHOR'S BIOGRAPHY



Jim Williams is a staff scientist at Linear Technology Corp ([www.linear.com](http://www.linear.com)), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys sports cars, art, collecting antique scientific instruments, sculpture, and restoring old Tektronix oscilloscopes.

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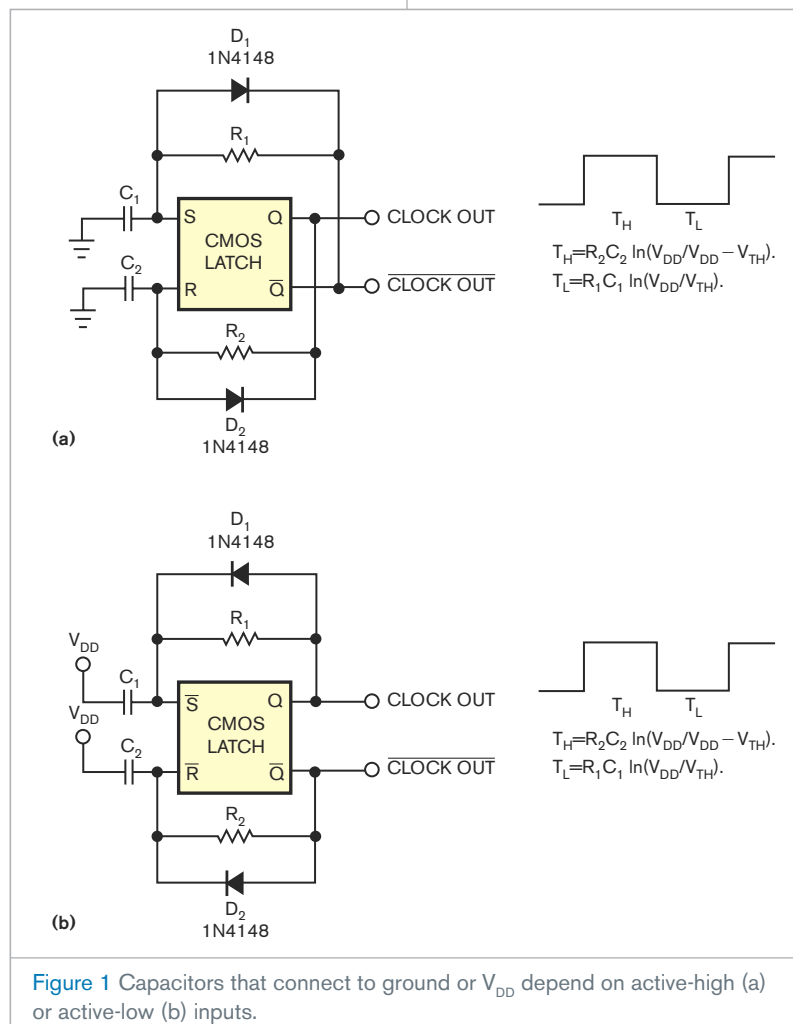
READERS SOLVE DESIGN PROBLEMS

## Turn a set/reset latch into an astable/monostable multivibrator

Luca Bruno, ITIS Henseberger Monza, Lissone, Italy

 This Design Idea describes a simple way to form a reliable astable or monostable multivibrator from a set/reset latch. You may find it useful because it lets you minimize the number of standard digital ICs your de-

sign requires when absolute precision isn't an issue. You can use a set/reset latch either with active-low or active-high inputs, which you can build with two NAND or NOR logic gates. You can also use integrated set/reset latches



**Figure 1** Capacitors that connect to ground or  $V_{DD}$  depend on active-high (a) or active-low (b) inputs.

### DIs Inside

45 555 timer eliminates LED driver's need for microprocessor control

46 Smart photoresistor timer needs few components

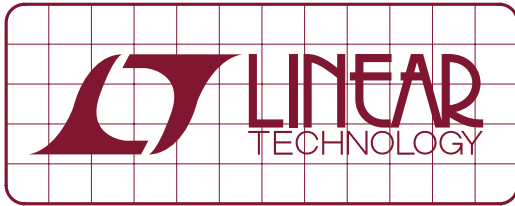
48 High-performance adder uses instrumentation amplifiers

50 Nonvolatile standby/on switch remembers its state

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or any type of flip-flop that comes with asynchronous preset and clear inputs because they have the same function as the set/reset inputs when the clock and data inputs are grounded. This method functions only with CMOS logic families that offer the benefits of high input impedance; a quasi-ideal voltage-transfer characteristic with a threshold voltage,  $V_{TH}$ , typically equal to the drain-to-drain voltage,  $V_{DD}$ , divided by two; and low power consumption. This concept has undergone testing with a 74HC00 quad NAND, a 74HC02 quad NOR, a CD4001 quad NOR, a CD4011 quad NAND, and a CD4013 dual-D-type flip-flop.

Connecting two RC networks between the complementary outputs Q and Q-bar and set and reset inputs enables astable operation (Figure 1). Due to complementary outputs, the circuit has no stable state, and it toggles continuously, generating an output clock. The time constants  $R_2 C_2$  and  $R_1 C_1$  set the high and low time periods,  $T_H$  and  $T_L$ , respectively, and also the duty cycle. Diodes  $D_1$  and  $D_2$  quickly discharge capacitors  $C_1$  and  $C_2$  so that, on the next



# DESIGN NOTES

## One Device Replaces Battery Charger, Pushbutton Controller, LED Driver and Voltage Regulator ICs in Portable Electronics

Design Note 470

Marty Merchant

### Introduction

The LTC<sup>®</sup>3577/LTC3577-1 integrates a number of portable device power management functions into one IC, reducing complexity, cost and board area in handheld devices. The major functions include:

- Five voltage regulators to power memory, I/O, PLL, CODEC, DSP or a touch-screen controller
- A battery charger and PowerPath™ manager
- An LED driver for backlighting an LCD display, keypad and/or buttons
- Pushbutton control for debouncing the on/off button, supply sequencing and allowing end-users to force a hard reset when the microcontroller is not responding

By combining these functions, the LTC3577/LTC3577-1 does more than just reduce the number of required ICs; it solves the problems of functional interoperability—where otherwise separate features operate together for improved end-product performance. For instance, when the power input is from USB, the limited input current is logically distributed among the power supply outputs and the battery charger.

The LTC3577/LTC3577-1 offers other important features, including PowerPath control with instant-on operation, input overvoltage protection for devices that operate in harsh environments and adjustable slew rates on the switching supplies, making it possible to reduce EMI while optimizing efficiency. The LTC3577-1 features a 4.1V battery float voltage for improved battery cycle life and additional high temperature safety margin, while the LTC3577 includes a standard 4.2V battery float voltage for maximum battery run time.

### Pushbutton Control

The built in pushbutton control circuitry of the LTC3577/LTC3577-1 eliminates the need to debounce the pushbutton and includes power-up sequence functionality. A PB

Status output indicates when the pushbutton is depressed, allowing the microprocessor to alter operation or begin the power-down sequence. Holding the pushbutton down for five seconds produces a hard reset. The hard reset shuts down the three bucks, the two LDOs and the LED driver, allowing the user to power down the device when the microprocessor is no longer responding.

### Battery, USB, Wall and High Voltage Input Sources

The LTC3577/LTC3577-1 is designed to direct power from two power supply inputs and/or a Li-Ion/Polymer battery. The  $V_{BUS}$  input has selectable input current limit control, designed to deliver 100mA or 500mA for USB applications, or 1A for higher power applications.

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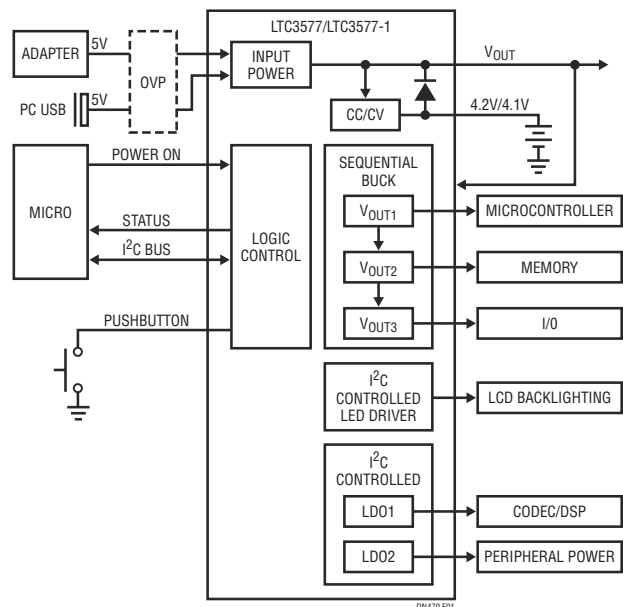


Figure 1. Portable Device Power Distribution Block Diagram Featuring the LTC3577/LTC3577-1

A high power voltage source such as a 5V supply can be connected via an externally controlled FET. The voltage control ( $V_C$ ) pin can be used to regulate the output of a high voltage buck, such as the LT3480, LT3563 or LT3505 at a voltage slightly above the battery for optimal battery charger efficiency.

Figure 1 shows a system block diagram of the LTC3577/LTC3577-1. An overvoltage protection circuit enables one or both of the input supplies to be protected against high voltage surges. The LTC3577/LTC3577-1 can provide power from a 4.2V/4.1V Li-Ion/Polymer battery when no other power is available or when the  $V_{BUS}$  input current limit has been exceeded.

### Battery Charger

The LTC3577/LTC3577-1 battery charger can provide a charge current up to 1.5A via  $V_{BUS}$  or wall adapter when available. The charger also has an automatic recharge and a trickle charge function. The battery charge/no-charge status, plus the NTC status can be read via the I<sup>2</sup>C bus. Since Li-Ion/Polymer batteries quickly lose capacity when both hot and fully charged, the LTC3577/LTC3577-1 reduces the battery voltage when the battery heats up, extending battery life and improving safety.

### Three Bucks, Two LDOs and a Boost/LED Driver

The LTC3577/LTC3577-1 contains five resistor-adjustable step-down regulators: two bucks, which can provide up to 500mA each, a third buck, which can provide up to 800mA, and two LDO regulators, which provide up to 150mA each and are enabled via the I<sup>2</sup>C interface. Individual LDO supply inputs allow the regulators to be connected to low voltage buck regulator outputs to improve efficiency. All regulators are capable of low-voltage operation, adjustable down to 0.8V.

The three buck regulators are sequenced at power up ( $V_{OUT1}$ ,  $V_{OUT2}$  then  $V_{OUT3}$ ) via the pushbutton controller or via a static input pin. Each buck can be individually selected to run in Burst Mode<sup>®</sup> operation to optimize efficiency or pulse-skipping mode for lower output ripple at light loads. A patented switching slew rate control feature, set via the I<sup>2</sup>C interface, allows the reduction of EMI noise in exchange for efficiency.

The LTC3577/LTC3577-1 LED boost driver can be used to drive up to 10 series white LEDs at up to 25mA or be configured as a constant voltage boost converter. As a LED driver, the current is controlled by a 6-bit, 60dB logarithmic DAC, which can be further reduced via internal PWM control. The LED current smoothly ramps up and down at one of four different rates. Overvoltage protection prevents the internal power transistor from damage if an open circuit fault occurs. Alternatively, the LED boost driver can be configured as a fixed voltage boost, providing up to 0.75W at 36V.

Many circuits require a dual polarity voltage to bias op amps or other analog devices. A simple charge pump circuit, as shown in Figure 2, can be added to the boost converter switch node to provide a dual polarity supply. Two forward diodes are used to account for the two diode voltage drops in the inverting charge pump circuit and provide the best cross-regulation. For circuits where cross-regulation is not important, or with relatively light negative loads, using a single forward diode for the boost circuit provides the best efficiency.

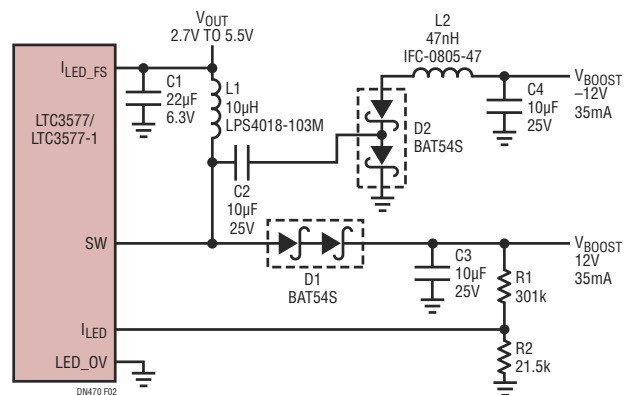


Figure 2. Dual Polarity Boost Converter

### Conclusion

The high level of integration of the LTC3577/LTC3577-1 reduces the number of components, required board real estate and overall cost; and greatly simplifies design by solving a number of complex power flow logic and control problems.

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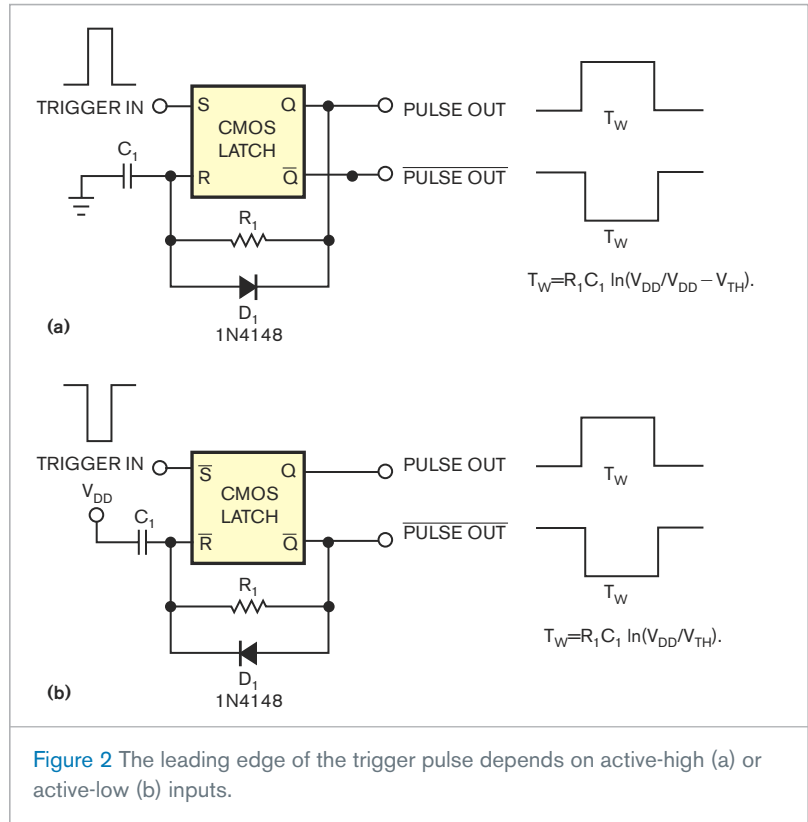
  
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cycle, they will recharge from 0V.

In monostable mode, connect one RC network (Figure 2), depending whether you need a positive-pulse or a negative-pulse trigger. When an input trigger pulse occurs, it sets the output pulse,  $T_W$ , which remains in this state until the RC network activates the reset pin. The RC time constant sets the output-pulse width. For correct operation, the trigger pulse must be shorter than the output pulse. Diode  $D_1$  reduces recovery time.

The threshold voltage has the typical value  $V_{DD}/2$ , but it may change from 0.33 to 0.67 of  $V_{DD}$  for the CD4000 CMOS family. The parameters of the generated output signals of the circuits in figures 1 and 2 present variations from unit to unit as a function of threshold-voltage shift. On the other hand, the threshold voltage presents good stability with supply voltage and temperature variations.

For best accuracy, the timing capacitors for both astable and monostable circuits should be nonpolarized, have low leakage, and be much larger than the inherent stray capacitance in the circuit, and the timing resistors for both astable and monostable circuits must be much larger than the



CMOS on-resistance in series with them, which typically is hundreds of ohms. In addition, you must decouple

the supply voltage for safety to prevent voltage spikes, which may disturb the circuits. **EDN**

## 555 timer eliminates LED driver's need for microprocessor control

Michael Day, Texas Instruments, Dallas, TX

LEDs find their way into applications that range from high-end video displays to low-end lighting applications. Designers often need only some of the functions of a dedicated LED driver but can't afford the cost

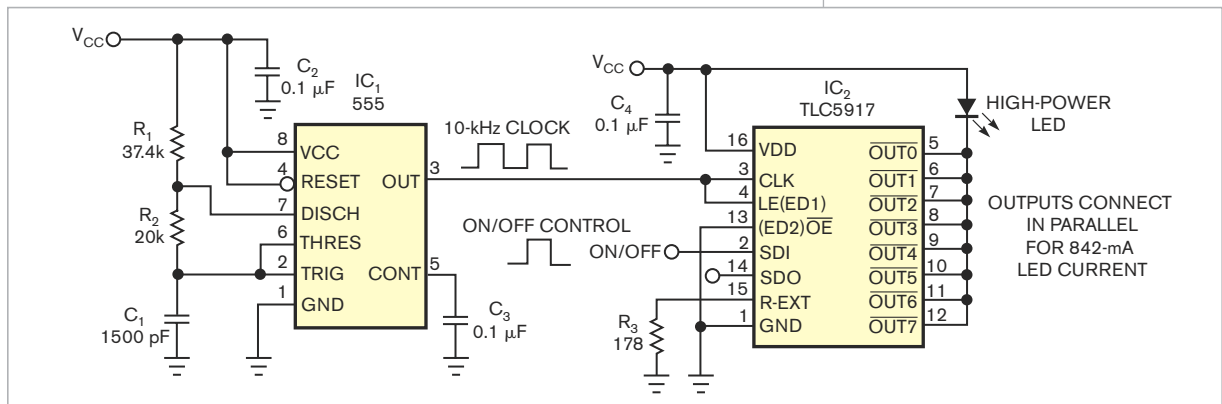


Figure 1 A 555 timer provides the necessary pulses for configuring an LED driver.

of the microprocessor to control them. Microprocessors typically control dedicated LED drivers, enabling features such as analog or PWM (pulse-width modulation) for LED-current control, independent control of each LED, and reading LED status and faults. If your design requires a constant-current LED, such as those in LED lighting or luminaires, then you may not need these advanced features. In these applications, a 555 timer can replace the microprocessor and still allow accurate control of LED current independently of input voltage, temperature, and LED forward-voltage drops.

IC<sub>2</sub>, a TLC5917 dedicated LED driver, controls eight independent constant-current sinks (Figure 1). It normally requires a microprocessor to drive four digital-input signals. The command  $\overline{OE}$  (output enable) enables and disables the IC. Data on the SDI (serial-data-input) pin clocks into the IC's input shift registers on the rising edge of the clock. The data in the shift registers transfers into internal on/off latches on the falling edge of the LE (latch).

Either the TLC5917 outputs can drive eight independent LEDs, or you can parallel its outputs to increase the current to drive one higher-power LED. Its internal current-setting registers have default values at start-up. These values, along with external current-setting resistor  $R_3$ , set the LED current. In this application,  $R_3$  sets each output's current to 105 mA:  $18.75V/R_3 = 18.75A/178\Omega$ . Connecting all outputs in parallel yields 842 mA of LED current.

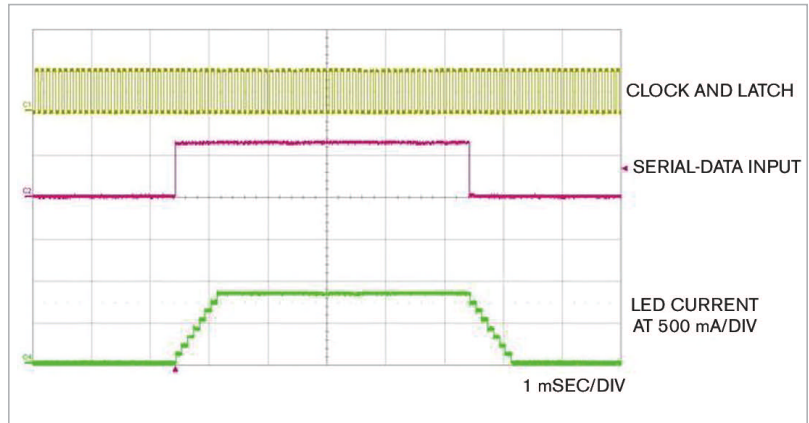


Figure 2 The LED current (lower trace) ramps up and down in eight steps.

At power-up, the internal on/off latches that turn each output on or off default to zero, so you must set these latches to one before the outputs turn on. The 555 timer replaces the microprocessor for this function. The clock and latch lines both connect to the 555 timer's square-wave output. At each rising edge of the clock, the SDI shifts into the TLC5917's input shift register. This data latches into the on/off latch at the falling edge of the latch signal. Because shifting the data and latching the data occur at different clock edges, the clock and latch pins can connect to the same input clock signal. Hard-wiring  $\overline{OE}$  to ground permanently enables the IC. You can connect SDI to the power-supply voltage to automatically turn on the LED at power-up. This connection continuously clocks in ones to turn on all outputs. You can also connect SDI to a switch or a digital input to allow for LED on/off control. Then, SDI

can pull to the power-supply voltage, which continuously clocks in all ones to turn on the outputs. Alternatively, it can pull to ground, which continuously clocks in all zeros to turn off the outputs.

The 555 timer's clock speed determines how fast the LEDs turn on and off. The LED current ramps from 0 to 100% in eight clock pulses as each falling edge of the latch pin latches the SDI data into another of the eight internal on/off latches, turning on or off another one of the eight outputs. Figure 2 shows the resulting stair-stepped LED current increasing and decreasing with each successive falling edge of the latch. Even a relatively low clock speed of 10 kHz results in an on/off transition of only 0.8 msec, which the human eye perceives as instantaneous. You can achieve gradual turn-on and turn-off with low clock speeds. Setting the clock to 0.1 Hz gradually turns the LED on and off in 0.8 sec. **EDN**

## Smart photoresistor timer needs few components

Abel Raynus, Armatron International Inc, Malden, MA

An application required a photo timer with some unusual functions. It had to switch on the load, a lamp, an hour after sunset. After working for three hours, the timer should turn the load off, which had to remain

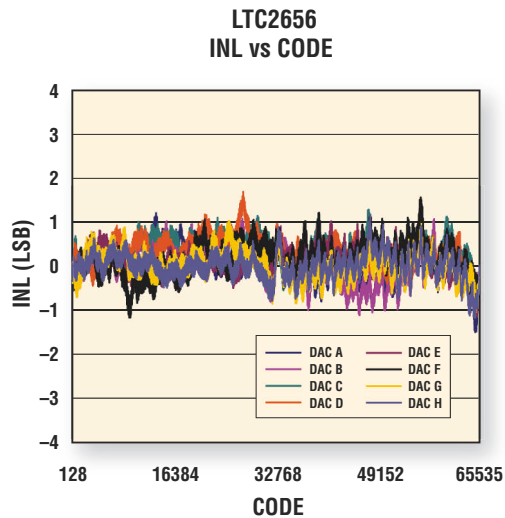
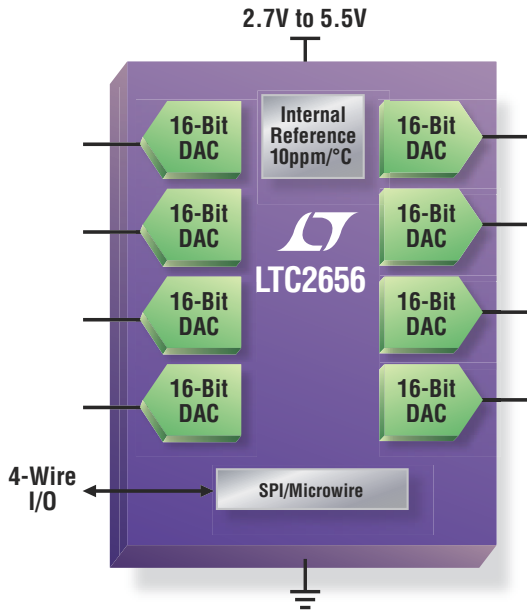
off until an operator manually reactivated the timer. The timer had to reside between the main 110/220V-ac line and the load. And, as with any other consumer product, it had to be cost-effective. You can achieve these

goals by using a voltage comparator and dual timers with an RC-timing network, but an inexpensive, 8-bit microcontroller with a built-in ADC provides a more elegant approach. You can perform all the functions in firmware. Listing 1, which is available at [www.edn.com/090903dia](http://www.edn.com/090903dia), contains downloadable source code.

Figure 1 shows the circuit, which uses an eight-pin MC68HC908QT2 microcontroller from Freescale Semi-



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LTC2657-12	12	I <sup>2</sup> C	8
LTC2654-16*	16	SPI	4
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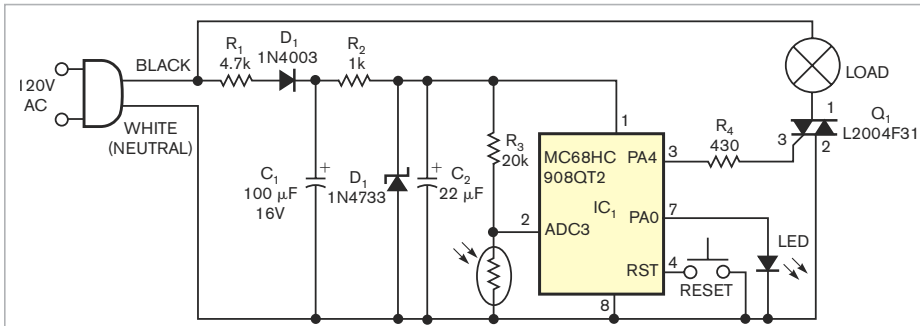


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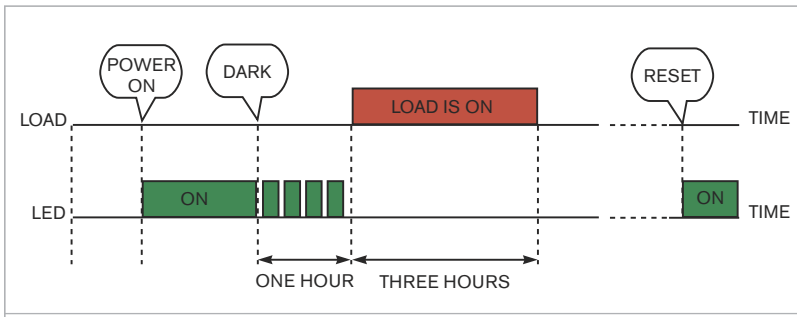
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**Figure 1** This circuit uses an eight-pin microcontroller and a logic switch to provide a smart photoresistor.



**Figure 2** The LED is on when the timer is ready for work and waits for darkness. It blinks during the delay, and it is off when the timer waits for reactivation.

current and main voltage. The L2004F31 requires only 3 mA of dc-gate-trigger current, and it conducts 4A rms at 200V ac. The VT90N1 photoresistor from PerkinElmer ([www.optoelectronics.perkinelmer.com](http://www.optoelectronics.perkinelmer.com)) has a dark resistance of 200 k $\Omega$ , which drops in light to 10 k $\Omega$  or less. The LED indicates the status of the timer: It is on when the timer is ready for work and waits for darkness. It blinks during the delay, and it is off when the timer waits for reactivation (**Figure 2**). The W934GD5V LED from Kingbright ([www.kingbright.com](http://www.kingbright.com)) has a built-in resistor that minimizes the number of necessary components. To reactivate the timer, press the pushbutton reset switch. All time delays are set in firmware, and you can easily change them.**EDN**

**REFERENCE**

- 1 Raynus, Abel, "AC line powers microcontroller-based fan-speed regulator," *EDN*, Nov 9, 2006, pg 128, [www.edn.com/article/CA6387025](http://www.edn.com/article/CA6387025).

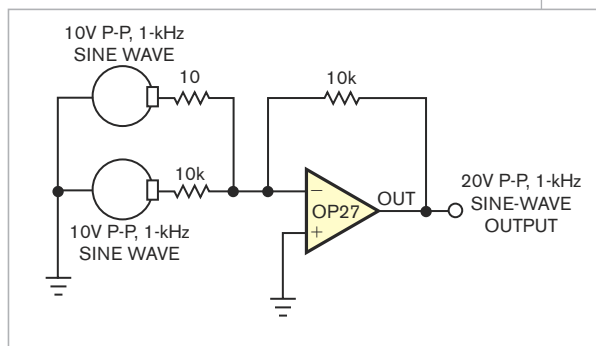
conductor ([www.freescale.com](http://www.freescale.com)). **Reference 1** describes a microcontroller's power supply. Q<sub>1</sub>, an L2004F31 logic

triac from Littelfuse ([www.littelfuse.com](http://www.littelfuse.com)), switches the load on and off; the type you use depends only on the load

## High-performance adder uses instrumentation amplifiers

Moshe Gerstenhaber and Michael O'Sullivan, Analog Devices, Wilmington, MA

As instrumentation amplifiers become less costly, they can provide improved performance in applications that operational amplifiers traditionally served. The op-amp adder in **Figure 1** has a few shortcomings. First, the inputs have low to medium input impedance, which the input resistor of each signal determines. This arrangement causes gain errors when



**Figure 1** A typical adder configuration uses a single op amp.

the source impedance of the driving signal is large or requires the design of low-impedance driving sources. This circuit also has no common-mode-rejection capability, so inputs must be single-ended. The channel with the largest gain limits the performance of the entire system. Higher gain on one channel results in lower bandwidth, higher distortion, and increased system noise on all channels. To limit these effects, even low-performance adders require high-performance, high-bandwidth op amps.

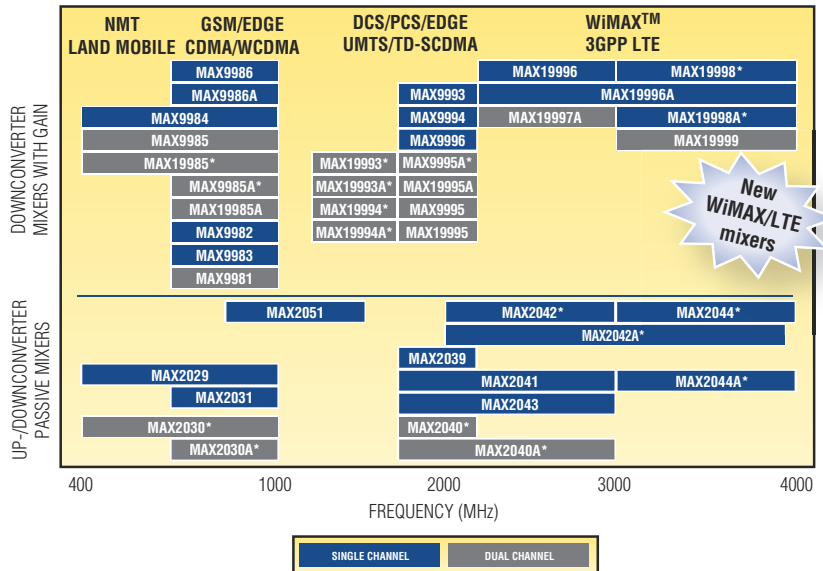
The noise gain of this op-amp adder is  $1 + 10,000 / (10 \parallel 10,000)$ . The input signal with the highest gain and 10 $\Omega$  input dominates the noise gain, but all inputs suffer increased offset voltage, gain error, noise,



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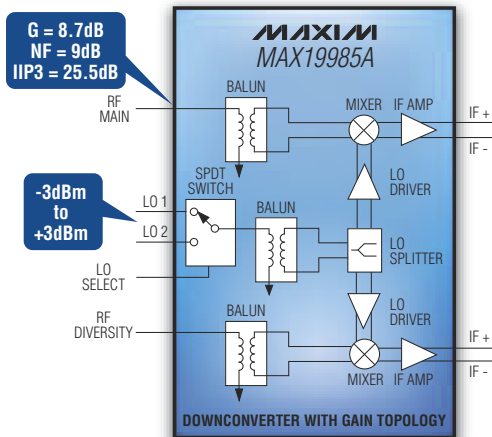
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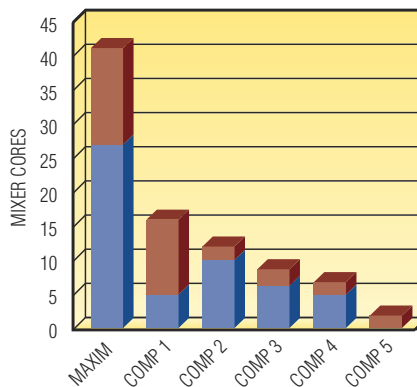


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and distortion. You can increase input impedance and improve common-mode rejection by using instrumentation amplifiers. The output voltage of an instrumentation amplifier is proportional to the voltage difference between the positive and the negative inputs. You can amplify this signal by connecting a resistor,  $R_{GAIN}$ , to the  $R_G$  pins (Figure 2). The output voltage is generated between the reference pin and the output pin. This arrangement allows you to use the reference pin to cascade multiple signals together in an adder configuration. You can set each instru-

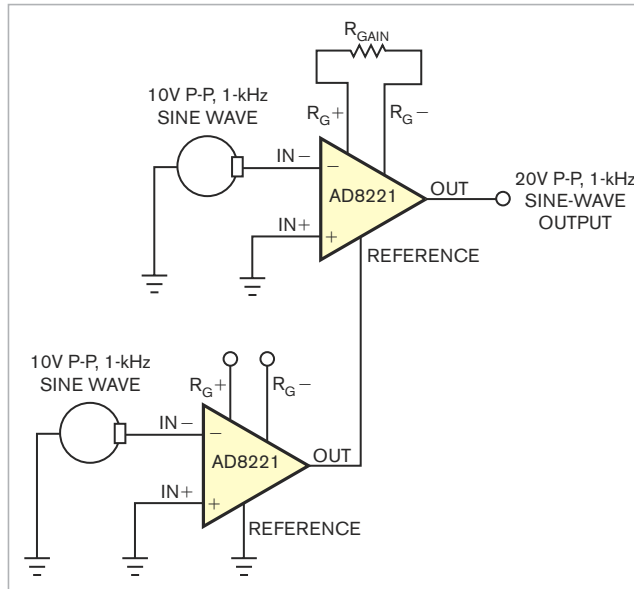


Figure 2 Two instrumentation amplifiers provide increased input impedance in this adder circuit.

mentation amplifier to a different gain.

This system has several advantages over the simple op-amp adder. For example, each input has extremely high input impedance and has independent common-mode rejection, which the instrumentation amp connected to that channel determines. The higher the channel gain, the higher the common-mode rejection, and the smaller the resulting error. You can also easily add or subtract signals by using the inverting or non-inverting terminals of the instrumentation amplifier, and the amplifier enables the use of differential input signals if you wish. Further,

the distortion, noise gain, and bandwidth of each signal are independent of the other signals, leading to lower offset voltage, gain error, noise, and distortion. Figure 3's THD+N (total-harmonic-distortion-plus-noise) plot demonstrates five times less distortion for the instrumentation-amplifier adder than that of the op-amp adder, even though the instrumentation amplifier has 1-MHz bandwidth and operates at 1 mA, whereas the op amp has 8-MHz bandwidth and operates at 4.5 mA. EDN

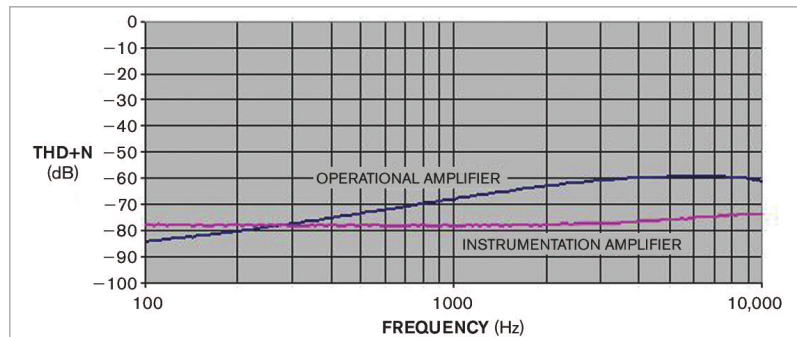


Figure 3 The instrumentation-amplifier configuration shows improved THD+N at frequencies greater than 300 Hz.

## Nonvolatile standby/on switch remembers its state

Anatoly Andrushevich, Maxim Integrated Products Inc, Moscow

You can use the standby/on switch in Figure 1 for industrial or telecom applications in which the circuitry must somehow “remember” its state—standby or on—after a power failure that occurs when no operator is present. An alternative approach uses a battery or a supercapacitor and a flip-flop. This approach is less reliable, however, because the cir-

cuit can lose its state if leakage current drains the battery. Another alternative involves the use of a microcontroller and EEPROM, but that approach requires software plus a provision for start-up time. Also, a stand-alone EEPROM for this application has an awkward interface.

You can use an electronically programmable voltage reference,  $IC_4$ , as a

single-bit nonvolatile-memory cell. To remember the state of the standby/on switch, this circuit programs  $IC_4$ 's output voltage high or low and can reprogram it at least 50,000 times.  $IC_1$  is a low-dropout linear regulator with reset output and a wide input-voltage range that extends to 72V. A microprocessor supervisor,  $IC_2$ , debounces the standby/on pushbutton and supports the programming of  $IC_4$  by increasing the pause length between pulses.  $IC_4$ 's output drives  $IC_5$ , an inverter with Schmitt-trigger input, which in turn drives the gate of transistor  $Q_2$  to control the main power supply.



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Flip-flop IC<sub>3</sub> helps to change the standby/on state with each press of the control button. At the end of IC<sub>4</sub>'s programming cycle, a low-to-high edge at IC<sub>3</sub>'s clock input sets the flip-flop to its opposite state, thanks to the feedback from the inverter. IC<sub>2</sub>'s reset triggers this action at power-up to ensure that the switch is ready to change state. Transistor Q<sub>1B</sub> and IC<sub>1</sub>'s reset output prevent the programming of incorrect states by blocking IC<sub>4</sub>'s adjust input during start-up and power-fail conditions.

You must block the effect of IC<sub>2</sub>'s power-up or -down reset pulse on IC<sub>4</sub>'s adjust input; C<sub>2</sub> therefore

sets IC<sub>2</sub>'s reset time-out to be longer than IC<sub>2</sub>'s reset time-out. The threshold voltage of IC<sub>2</sub>, 2.9V, is also lower than that of IC<sub>1</sub>, 4.6V. The worst-case

1.32V input-threshold voltage of IC<sub>5</sub> guarantees the standby position at first power-on because the factory-preset output for IC<sub>4</sub> is only 1.2V. **EDN**

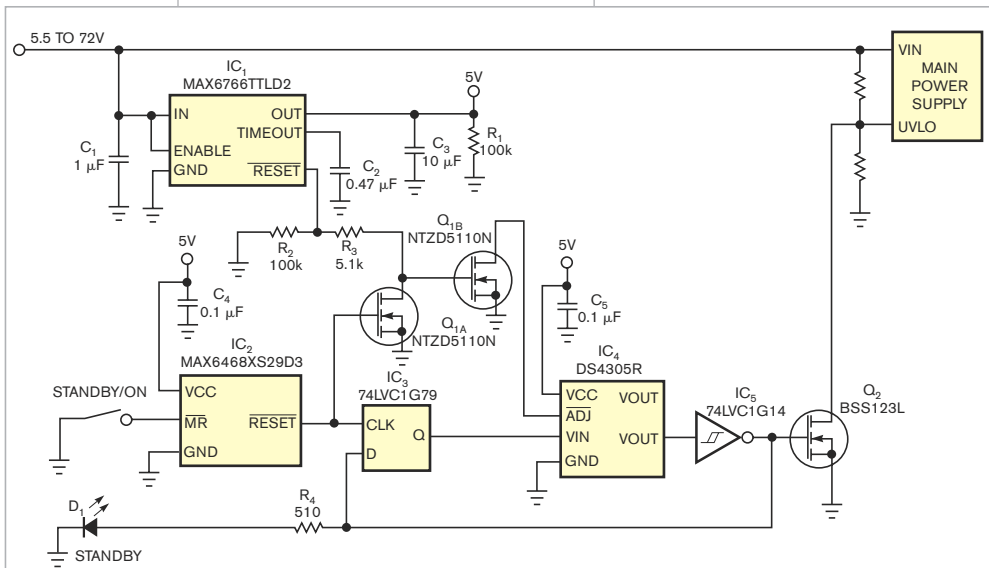


Figure 1 The circuit remembers its standby or on state if power fails with no operator present.

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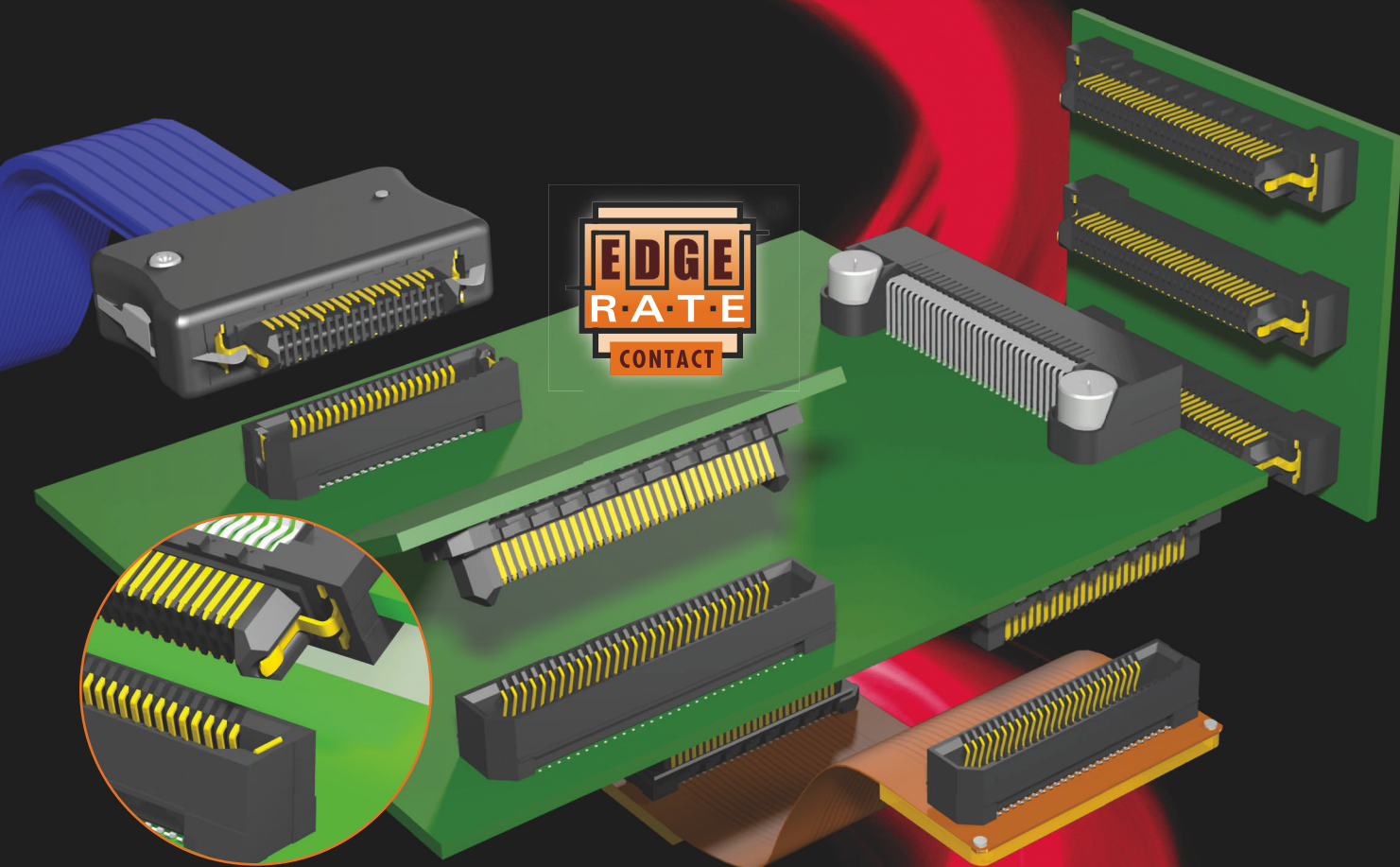


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# supplychain

LINKING DESIGN AND RESOURCES

## Distributors tap social media for designers

As more and more EEs look to the Web as an information source and for idea exchanges, electronics-component distributors are increasingly providing resource portals and e-communities for the engineers they serve. "The first thing we look at is how to reach out to design engineers and purchasers in a way that's meaningful and not intrusive," says Tony Harris, vice president of e-commerce at Digi-Key Corp ([www.digikey.com](http://www.digikey.com)). "Social marketing is a valuable vehicle for that [scenario] because it allows them to talk on their own terms."

Harris and company recently launched TowerGeeks.org, an online community that Digi-Key created for engineers that focuses on Freescale Semiconductor's ([www.freescale.com](http://www.freescale.com)) Tower System, a



modular, reconfigurable development platform for 8-, 16-, and 32-bit microcontrollers. The community invites members to discuss related projects, share and view videos, and tune into forums and groups. TowerGeeks.org also aims to supply unbiased information and services.

"Instead of pushing information out to the customer, they consume it in the way they want to consume it," Harris says. "We want to be a part of the conversation. Our goal isn't to interject into that conversation but to supply what's requested: a reliable resource of information."

PremierFarnell ([www.premierfarnell.com](http://www.premierfarnell.com)) and its businesses, Newark, Farnell, and Premier Electronics, also take an unbiased approach to their social-media activity, which their recent sponsorship of Element14 ([www.element-14.com](http://www.element-14.com)) illustrates. Based on Web 2.0 and offering an array of product data, design tools, and technology information, Element14 encourages engineers to participate in the community by posting comments, podcasts, and videos on design.

"We'd been looking at how to engage with the engineering community more deeply," says Jeff Hamilton (photo), director of marketing, design engineering, at Newark. "This site was going to be about what designers want: access to information in a very timely fashion."

## PICO PROJECTORS SET TO GROW

OUTLOOK

### Tiny pico projectors

embedded into products such as smartphones are set for a 60-fold increase in shipments during the next four years, according to iSuppli Corp ([www.iSuppli.com](http://www.iSuppli.com)). The market-research company estimates that shipments of embedded pico projectors—front projectors weighing less than 2 lbs and smaller than 60 in.<sup>3</sup> without a battery pack—will rise to more than 3 million units in 2013, up from less than 50,000 units this year.

"Mobile electronic devices offer consumers and corporate users the portability they desire, causing an increasing number of users to employ products like smartphones and netbook PCs as their primary platforms for computing and Internet access," says Sanju Khatri, principal analyst for signage and projection at iSuppli. "However, a major obstacle blocking the use of mobile devices in this fashion has been their tiny displays ... Embedded pico projectors promise to enlarge these displays, making mobile devices more capable as primary computing and Internet-access platforms."

Pico projectors are likely to find initial acceptance in the corporate market. However, iSuppli believes consumers will also be attracted to the technology.

### GREEN UPDATE

## INDUSTRY GROUPS FIGHT NEW YORK E-WASTE REGULATION

The CEA (Consumer Electronics Association, [www.cea.org](http://www.cea.org)) and the ITI (Information Technology Industry Council, [www.itic.org](http://www.itic.org)) have filed a legal challenge against New York City plans that would mandate manufacturers to provide free, door-to-door electronics collection to city residents. New York began promoting the required-electronics-recycling regulation in February 2008. In doing so, the city cited a report by the Environmental Protection Agency that estimated city residents buy almost 12 million electronic devices, or 92,000 tons of electronics, every year.

Estimates suggest the requirements will cost manufacturers more than \$200 million



annually, possibly resulting in cost increases to consumers and job losses. "Manufacturers recognize that they have a key role in providing recycling opportunities for consumers," says Gary Shapiro (photo), president and chief executive officer of CEA. "However, they do not have the only role. The responsibilities and costs for electronics recycling should be shared among all stakeholders, including city and state governments, retailers, recyclers, and consumers."

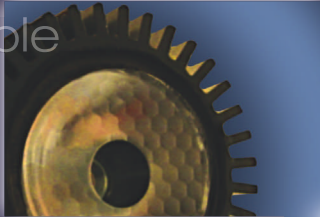
The law was scheduled to go into effect on July 31, but New York has agreed to delay all requirements of the e-waste program pending a decision on the preliminary injunction.



# Design with Light

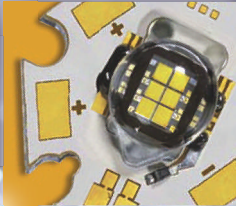


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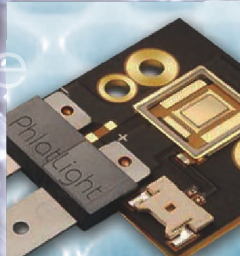


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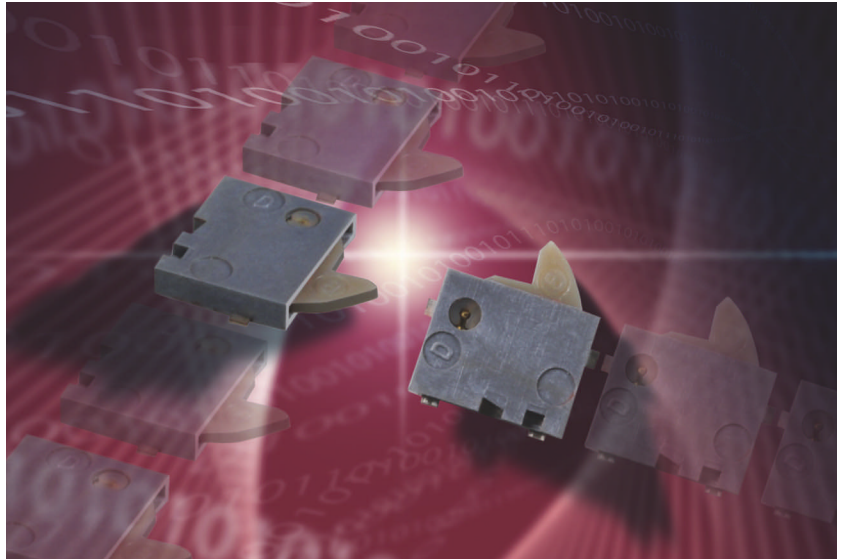
# productroundup

## SWITCHES AND RELAYS

### Side-actuated detection switch has 1.9-mm profile

↘ The microminiature GDS series side-actuated detection switches have a 1.9-mm profile and allow actuation from X or Y axes. Features include a 30g maximum actuation force, a 1-mA contact rating at 5V dc with a 1Ω maximum initial-contact resistance, and a 100-MΩ minimum insulation resistance between contacts. The device has a 100,000 minimum mechanical and electrical cycle and a -20 to +70°C temperature range. The GDS series costs 52 cents (10,000).

**C&K Components,**  
[www.ck-components.com](http://www.ck-components.com)



### Miniature circuit breaker has 14-kA short-circuit-interruption capacity

↘ The 17.5-mm-wide UL489 ac molded-case circuit breaker comes in a 20A C trip curve. Features include a 14-kA short-circuit-interrupting capacity, a green/red positive-trip indicator, and an HVACR 40°C rating. Suiting wiring protection, power supplies, transformers, and industrial controls, the breaker allows easy DIN-rail mounting. Available in single-pole versions, the UL489 ac miniature mold-case circuit breakers cost \$39.

**Altech,** [www.altechcorp.com](http://www.altechcorp.com)

### Illuminated tactile switches provide cap-style and color options

↘ The JB illuminated subminiature tactile-switch series provides full-face illumination in red, green, or yellow LEDs with cap styles and colors, including flat translucent, flat with lens and diffusers, or button-framed. The 10-mm switches have a rubber-seal construction, preventing contact contamination and allowing automated soldering and cleaning. Slanted terminals enable a spring-type action, allowing secure PCB mounting and preventing dislodging during wave soldering. The devices can perform a minimum of 5 million operations, and their terminal spacing conforms to a 2.54-mm PCB grid. The SPST switches have a momentary circuit and a 50-mA rating at a maximum 24V dc for standard-operating-force models and a 125-mA rating at a maximum 24V dc for high-operating-force models. Operating over a -25 to +70°C temperature range, the JB illuminated tactile-switch series costs \$1.53 (2500).

**NKK Switches,** [www.nkkswitches.com](http://www.nkkswitches.com)

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dles cost \$427.50 and \$843, respectively. **Kingston Technology**, [www.kingston.com](http://www.kingston.com)

### 24-in. LCDs use SpectraView color calibration

The MultiSync LCD2490WUXi<sup>2</sup> and the LCD2490W2-BK-SV 24-in. LCDs use the vendor's SpectraView color-calibration technology. Using X-Light Pro technology allows the displays to maintain consistent light output and correct for short-term fluctuations. The devices suit graphic arts, desktop publishing, photography, and medical imaging. Features include a 1900×1200-pixel native resolution, a 1000-to-1 contrast ratio, and 320-cd/m<sup>2</sup> brightness. The MultiSync LCD2490WUXi<sup>2</sup> and the LCD2490W2-BK-SV cost \$1099 and \$1299, respectively, with a four-year parts and labor warranty. **NEC Display Solutions**, [www.necdisplay.com](http://www.necdisplay.com)

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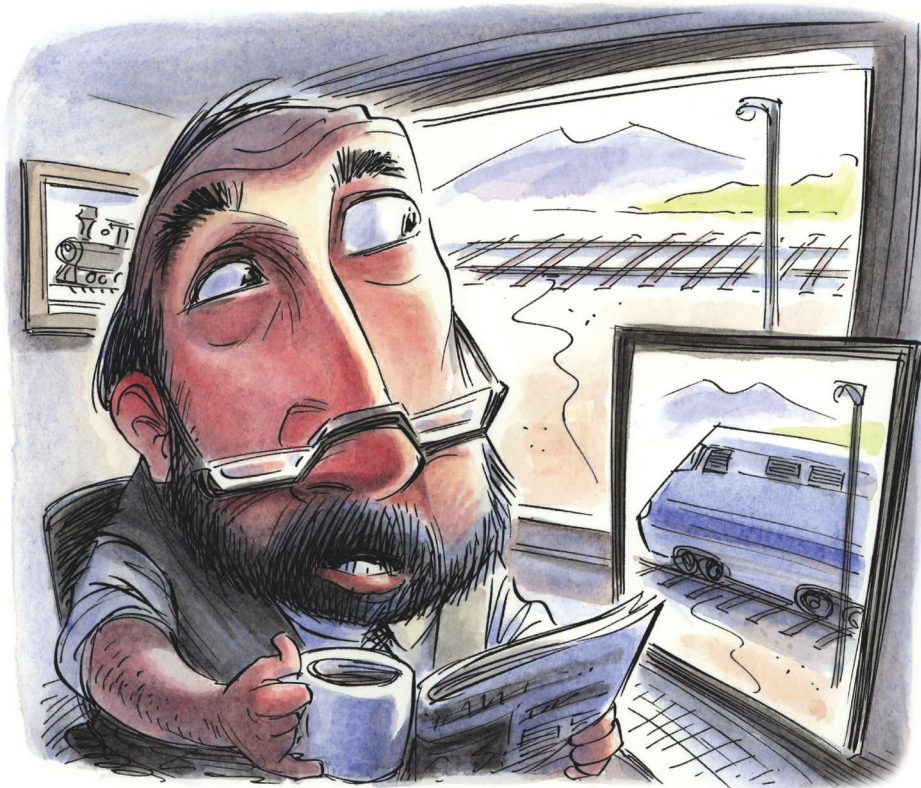
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## Unreal-wheel deal



**A** while ago, I got involved with troubleshooting a field issue on one of our wheel-sensing products. The product used inductive methods to sense the presence or absence of a train wheel. The inductive sensor would then drive an analog signal over twisted-pair copper wires from the sensing point to a central-processing location. The issue in this application was that the sensors were detecting phantom wheels.

The source of the problem was not obvious from initial clues and surface investigations. To troubleshoot, we started out by generating a diagram to map out all possible root causes. The one that seemed the most obvious, given the clues we had, was noise on the power supply to the sensor electronics. After isolating the power supply from the rest of the neighboring electronics and floating the supply from ground, we learned that the power supply was definitely not the cause of the phantom-wheel detections. We then became fixated on the local ground

reference for the central-processing system. We tested the ground and found it to be less than  $1\Omega$ —also not the problem.

We began to focus on capturing the actual waveforms coming into the central-processing system from the wheel sensors. We placed some analog data-acquisition modules on key signals coming from the wheel sensors. Once we captured the anomaly, we saw that there was a large noise disturbance on the analog signal after the signal was heavily filtered. Further dissection of the clues showed that the disturbances

coincided with a train's presence. We also noticed that the disturbances appeared to have a repetitive frequency of 100 Hz associated with them, as well. We began to suspect that we were seeing rectified noise from electric trains that used the overhead, 50-Hz electrification system for motive power. This idea sounded reasonable, but the question still remained about how this noise was getting into our system.

The system includes some heavy hardware and software filtering, such that any noise that could affect the system would have to be in-band with the wheel-detection signal, which was approximately 50 kHz. It is well-known that electric-train propulsion systems emit a broad band of harmonic frequencies. Was it possible that a 50-kHz component of these harmonics was magnetically coupling into our cables between the wheel sensors and the central-processing system? Our first reaction was that this scenario was not possible because we always used shielded cables and grounded the cable shield at the receiving end of the signal.

After weeks of frustration, I came across an old textbook stating that, when the cable length exceeds one-twentieth of a wavelength, you should ground both ends of the cable shield instead of just the receiver end. Just out of curiosity, I ran the calculation for one-twentieth of a wavelength for my signal at 50 kHz and determined it was 300m. Hmmm. Our cables in some cases could be as long as 2000m. Could it be that these recommendations and formulas that I had reserved in my mind for high-speed digital design applied to a much lower-frequency analog signal with a nearly one-mile-long cable?

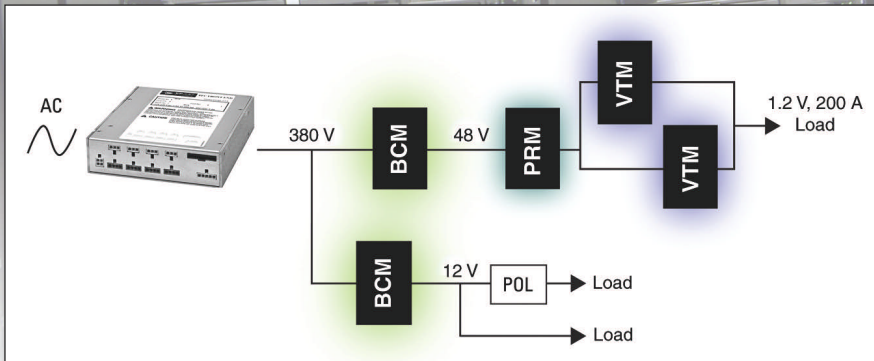
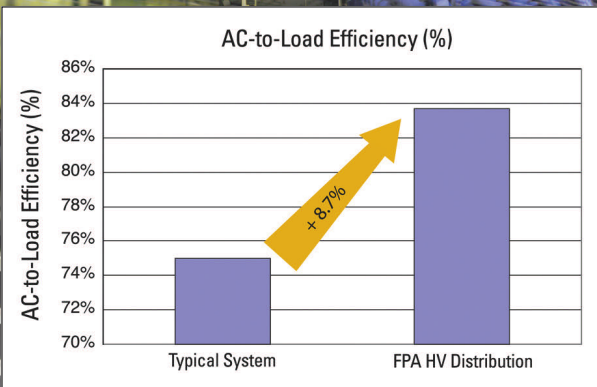
We modified the installations in which our cable lengths exceeded 300m to ground both ends of the cable shield, and we thus solved the problem. **EDN**

*Jeff Fries is a principal engineer and technologist for global signal technology at GE Transportation (Grain Valley, MO).*

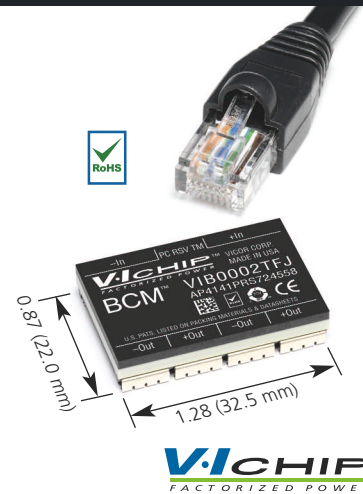
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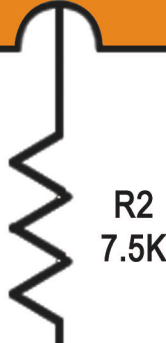


R1  
100K

What is the missing component?

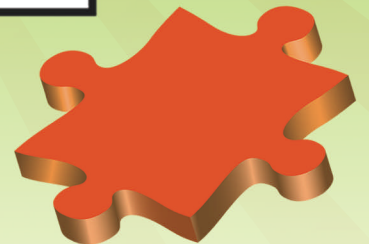


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